

SPECIFICATION



YMSG-G12864P-16DYSWWN

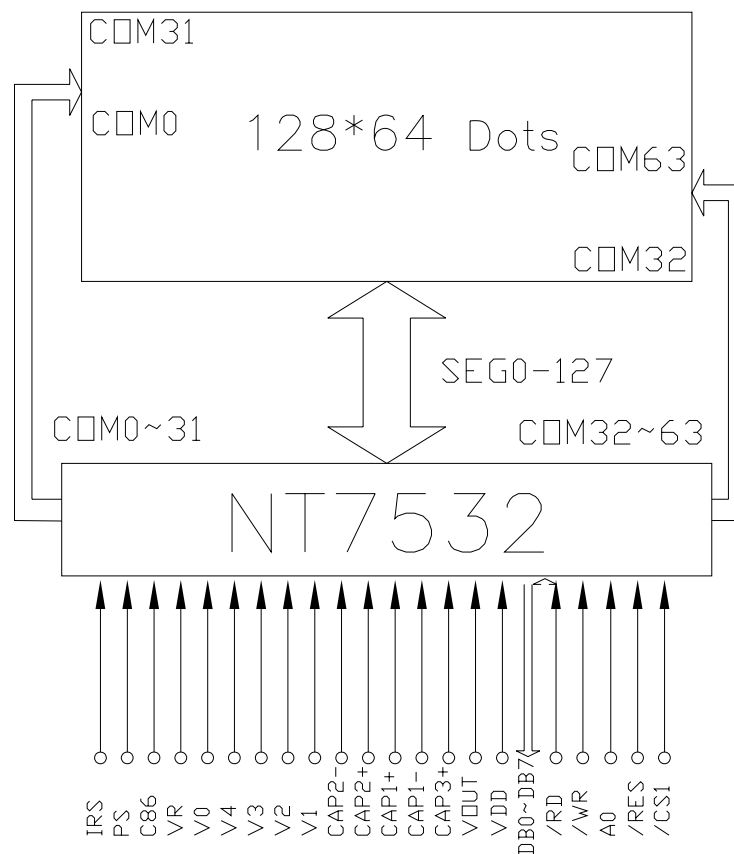
September 29, 2007
Version 1.01

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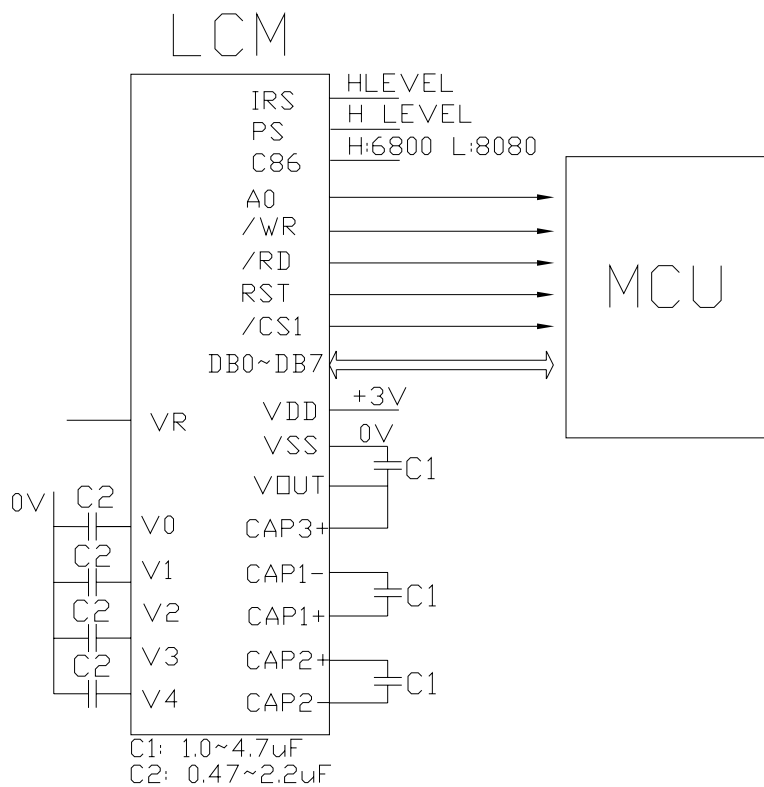
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1. FEATURES :

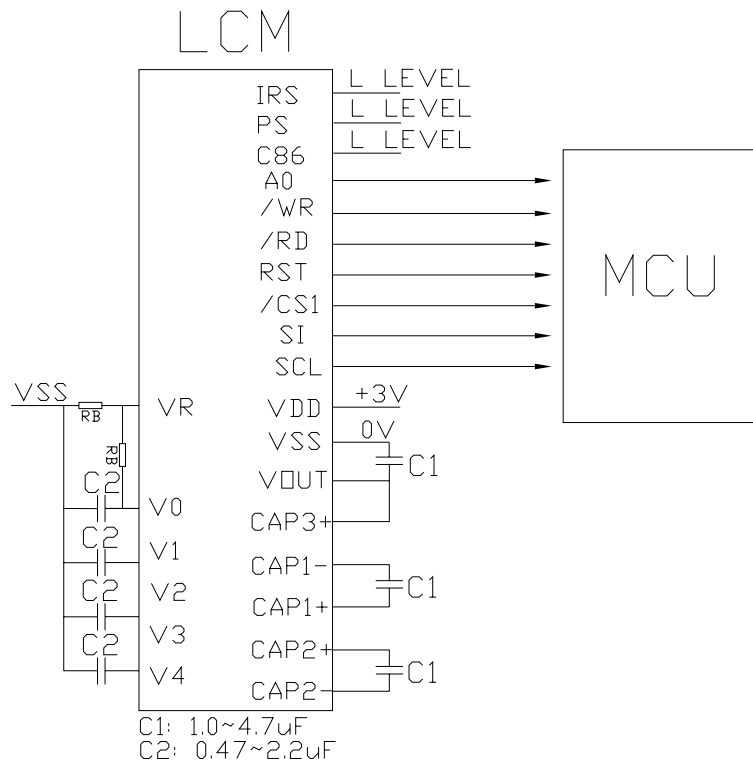
ITEM	STANDARD VALUE	UNIT
Display Type	128*64 dots	-
LCD Type	<input checked="" type="checkbox"/> YELLOW-GREEN, Transflective , Position <input type="checkbox"/> GREY, Transflective, Position <input type="checkbox"/> FSTN, Transflective , Position	-
LCD Duty	1/65	-
LCD Bias	1/9	-
Viewing Direction	6:00	-
Backlight Type	LED(WHITE)	-
Interface	6800/8080 series or Serial Interface	-
Driver IC	NT7532	-
Module Dimension	69.1(W) X50.0(H) X6.0 (MAX)(T)	mm
Effective Display Area	60.975 (W) X 32.935(H)	mm
Dot Size	0.45(W) X 0.49(H)	mm
Dot Pitch	0.475 W) X 0.515 (H)	mm

2. BLOCK DIAGRAM & APPLICATION CIRCUIT :


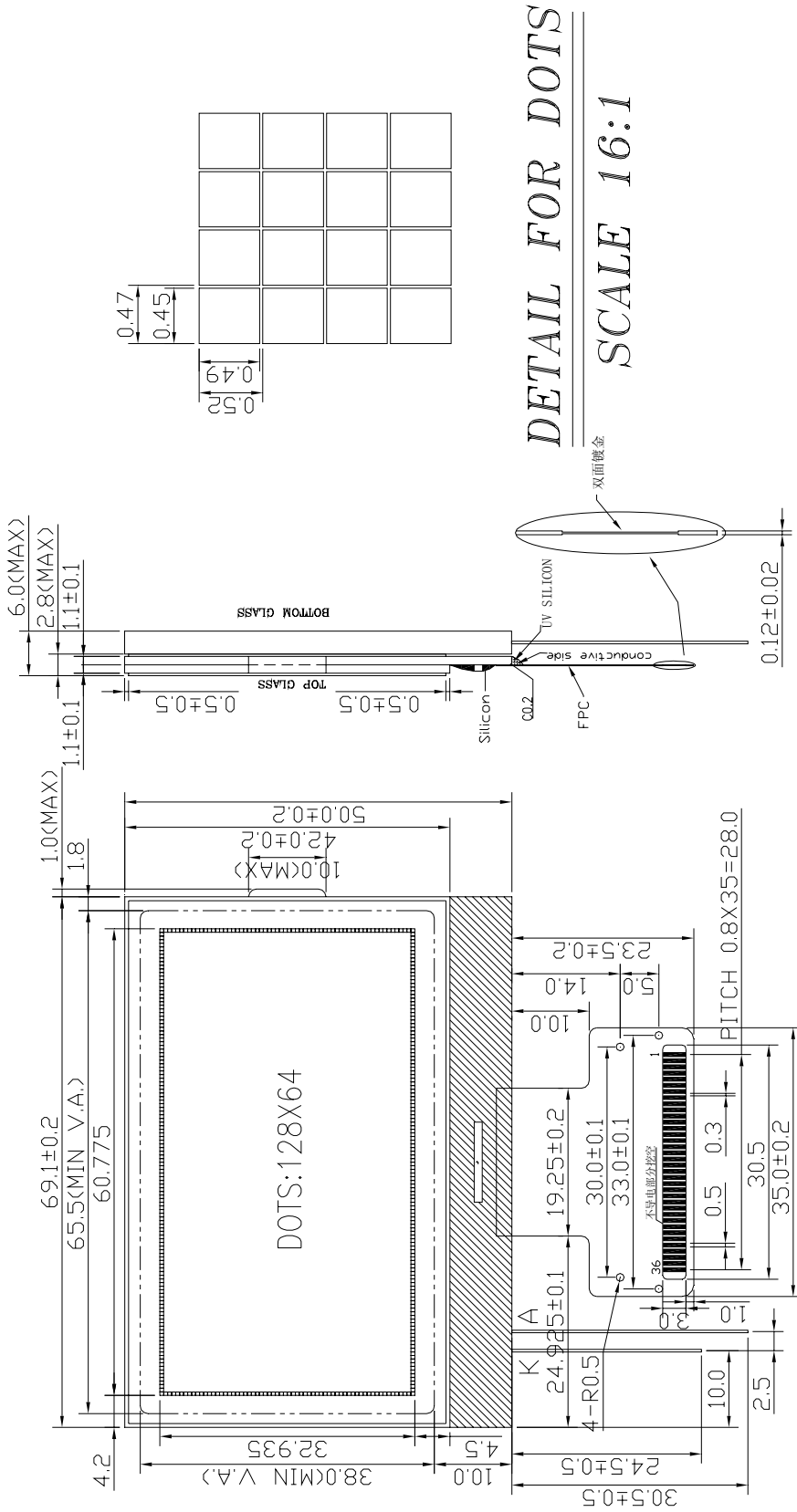
The Parallel Application(3X , internal resistor)



The Serial Interface Application(3X , external resistor)



3. OUTLINE DIMENSIONS



4. ABSOLUTE MAXIMUM RATING

ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
POWER SUPPLY FOR LOGIC	VDD	Ta=25°C	-0.3	—	3.6	V
INPUT VOLTAGE	VIN	Ta=25°C	-0.3	—	VDD+0.3	V
Module OPERATION TEMPERATURE	TOPR	---	-10	—	+60	°C
Module STORAGE TEMPERATURE	TSTG	---	-20	—	+70	°C
Storage Humidity	H _D	Ta < 40 °C	-		90	%RH

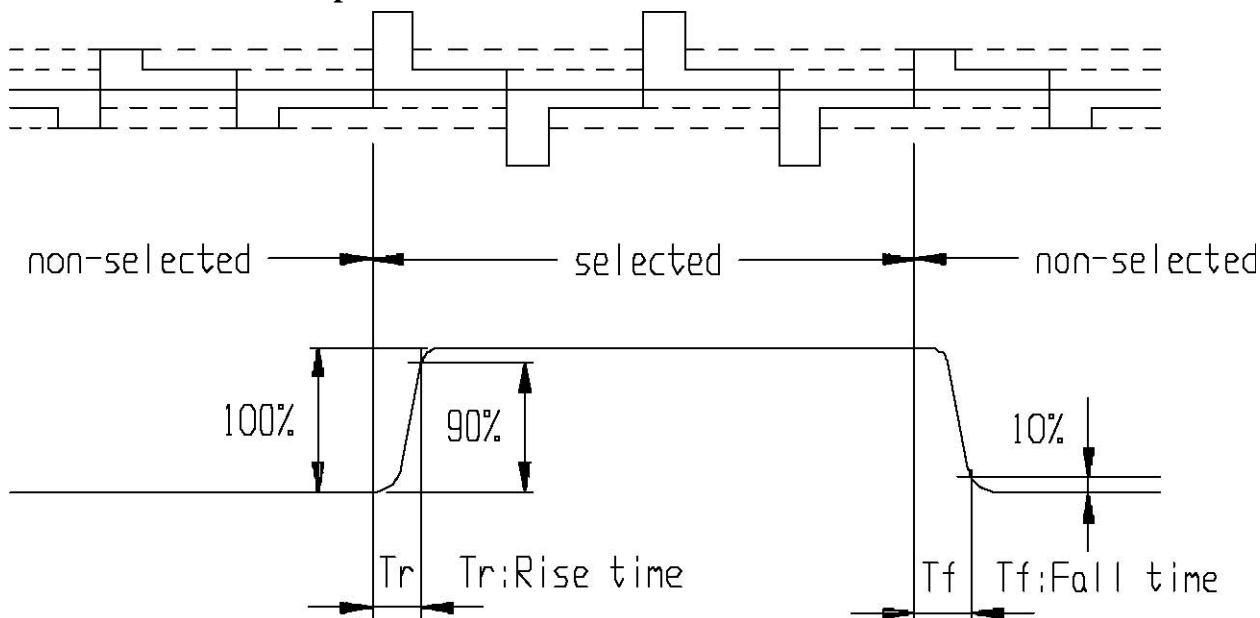
5. ELECTRICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Supply Voltage (logic)	VDD-VSS	-	2.4	3	3.5	V
Supply Voltage (LCD)	VDD-V0	Ta= +25°C	-	8	-	V
Input signal voltage	V-IH	“H” level	0.5VDD	-	VDD	V
	V-IL	“L” level	VSS	-	0.2 VDD	V
Output signal voltage	V-OH	“H” level	2.4	-	-	V
	VOL	“H” level	-	-	VSS+0.4	V
Supply Current (logic)	IDD	VDD=3.0V	-	-	225	μA
Backlight Voltage	V-BL	-	-	3.0	3.1	V
Backlight Current	I-BL	-		80-	90	mA
Backlight Driver Wave						kHz
Backlight Brightness						
Backlight Life Time						

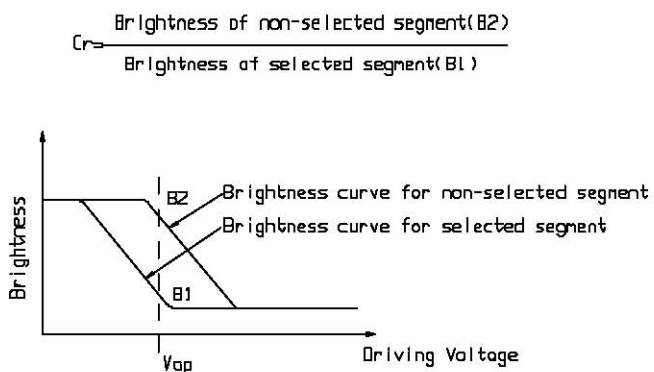
6. OPTICAL CHARACTERISTICS

Item	Symbol	Condition	Min	Typ	Max	Unit	Remarks	Note
Response Time	Tr	-	-	140	-	ms	-	1
	Tf	-	-	133	-	ms	-	1
Contrast Ratio	Cr	-	-	5.1	-	-	-	2
Viewing Angle Range	θ	$Cr \geq 2$	41	-	-	deg	$\theta = 90$	3
			38	-	-	deg	$\theta = 270$	3
			32	-	-	deg	$\theta = 0$	3
			19	-	-	deg	$\theta = 180$	3

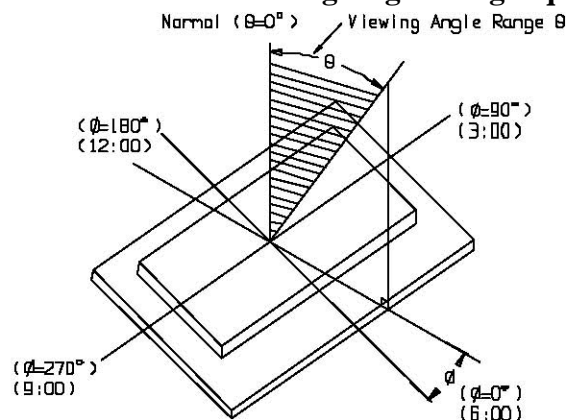
Note 1. Definition of response time



Note 2. Definition of Contrast Ratio 'Cr'



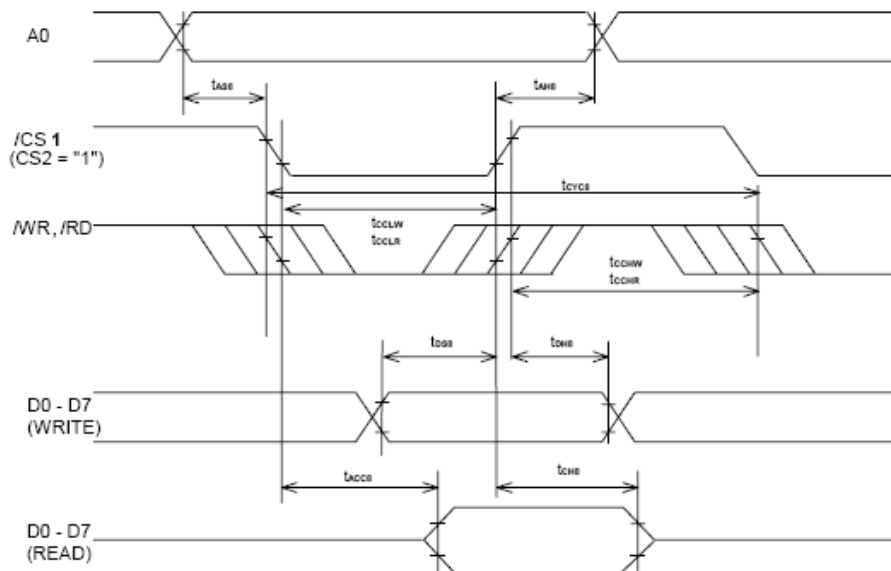
Note 3. Definition of Viewing Angle Range 'q'



7. TIMING CHARACTERISTICS

7.1 8080 Timing

System buses Read / Write characteristics 1 (For the 8080 Series MPU)



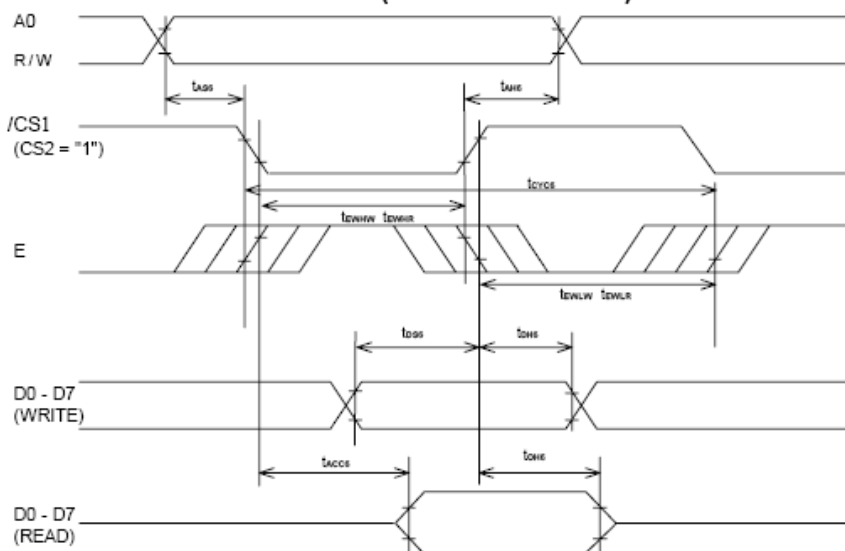
($V_{DD} = 2.4 - 3.5V$, $T_A = -40 - 85^\circ C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tAH8	Address hold time	0			ns	
tAS8	Address setup time	0			ns	
tCYC8	System cycle time	300			ns	
tCCLW	Control L pulse width (/WR)	90			ns	
tCCLR	Control L pulse width (/RD)	120			ns	
tCCHW	Control H pulse width (/WR)	120			ns	
tCCHR	Control H pulse width (/RD)	60			ns	
tDS8	Data setup time	40			ns	
tDH8	Data hold time	15			ns	
tACC8	/RD access time			140	ns	CL = 100pF
tCH8	Output disable time	10		100	ns	CL = 100pF

*1. The input signal rise time and fall time (t_r , t_f) is specified at 15ns or less. When the system cycle time is extremely fast, $(t_r+t_f) \leq (t_{CYC8}-t_{CCLW}-t_{CCHW})$ for $(t_r+t_f) \leq (t_{CYC8}-t_{CCLR}-t_{CCHR})$ are specified.

*2. All timing is specified using 20% and 80% of V_{DD} as the reference.

*3. tCCLW and tCCLR are specified as the overlap between CS1 being "L" (CS2 = "H") and /WR and /RD being at the "L" level.

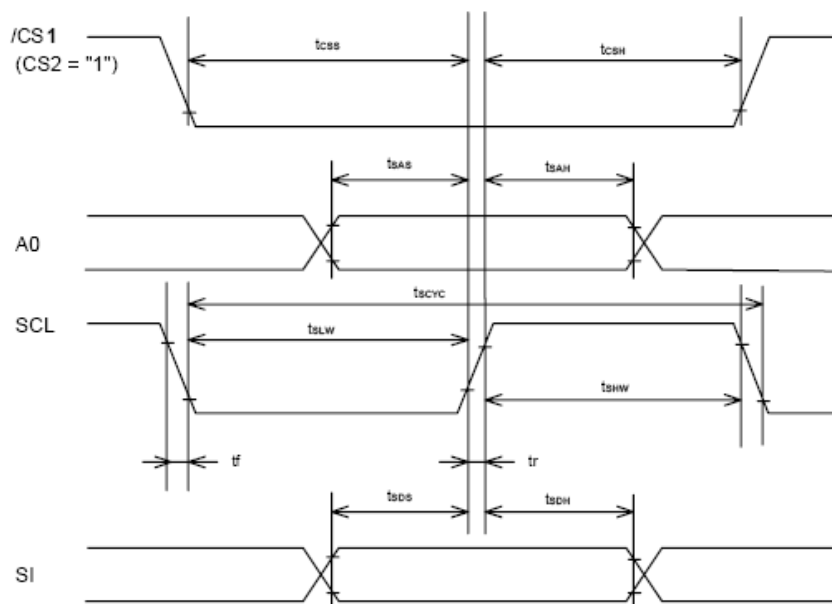
7.2 6800 Timing
System buses Read/Write Characteristics 2 (6800 Series MPU)

 $(V_{DD} = 2.4 - 3.5V, T_A = -40 - 85^{\circ}C)$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tCYC6	System cycle time	300			ns	
tAS6	Address setup time	0			ns	
tAH6	Address hold time	0			ns	
tDS6	Data setup time	40			ns	
tDH6	Data hold time	15			ns	
tOHR6	Output disable time	10		100	ns	$C_L = 100pF$
tOHL6	Output hold time			140	ns	$C_L = 100pF$
tEWHR	Enable H pulse width (Read)	120			ns	
tEWHW	Enable H pulse width (Write)	90			ns	
tEWLR	Enable L pulse width (Read)	60			ns	
tEWLW	Enable L pulse width (Write)	120			ns	

*1. The input signal rise time and fall time (t_r , t_f) is specified at 15ns or less. When the system cycle time is extremely fast, $(t_r+t_f) \leq (t_{CYC6}-t_{EWLW}-t_{EWHW})$ for $(t_r+t_f) \leq (t_{CYC6}-t_{EWLR}-t_{EWHR})$ are specified.

*2. All timing is specified using 20% and 80% of V_{DD} as the reference.

*3. tEWLW and tEWLR are specified as the overlap between /CS1 being "L" (CS2 = "H") and E.

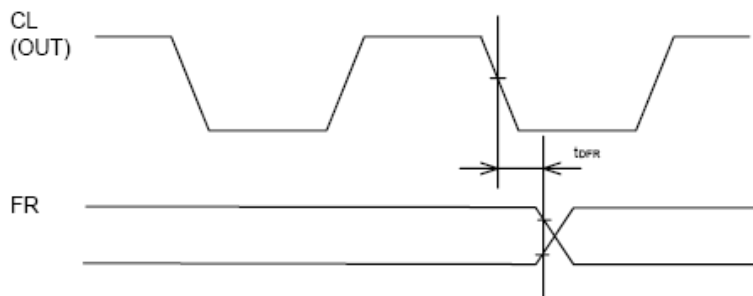
7.3 Serial Interface Timing
(1) Serial Interface


($V_{DD} = 2.4 - 3.5V$, $T_A = -40 - 85^{\circ}C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tSCYC	Serial clock cycle	250			ns	
tSHW	Serial clock H pulse width	100			ns	
tSLW	Serial clock L pulse width	100			ns	
tSAS	Address setup time	150			ns	
tSAH	Address hold time	150			ns	
tSDS	Data setup time	100			ns	
tSDH	Data hold time	100			ns	
tCSS	/CS serial clock time	150			ns	
tCSH	/CS serial clock time	150			ns	

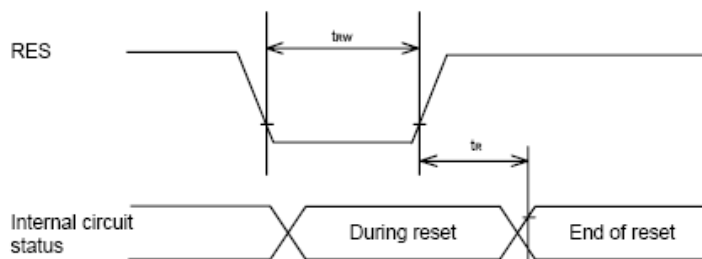
*1. The input signal rise time and fall time (t_r , t_f) are specified at 15ns or less

*2. All timing is specified using 20% and 80% of V_{DD} as the standard.

7.3 Display control and reset Timing
(2) Display Control Timing


($V_{DD} = 2.4 - 3.5V$, $T_A = -40 - 85^\circ C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tDFR	FR delay time		20	80	ns	$C_L = 50pF$

(3) Reset Timing


($V_{DD} = 2.4 - 3.5V$, $T_A = -40 - 85^\circ C$)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tR	Reset time			1.0	μs	
tRW	Reset low pulse width	1.0			μs	

8. DISPLAY CONTROL INSTRUCTION

Commands

The NT7532 uses a combination of A0, /RD(E) and /WR (R/W) signals to identify data bus signals. As the chip analyzes and executes each command using the internal timing clock only, regardless of the external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the /RD pad and a write status when a low pulse is input to the /WR pad. The 6800 series microprocessor interface enters a read status when a high pulse is input to the R/W pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics). Accordingly, in the command explanation and command table, (E) becomes 1(high) when the 6800 series microprocessor interface reads status of display data. This is the only different point from the 8080 series microprocessor interface.

Taking the 8080 series microprocessor interface as an example, commands are explained below.

When the serial interface is selected, input data starting from D7 in sequence.

Command Set

1. Display ON/OFF

Alternatively turns the display on and off.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	1	1	1	1	Display ON
										0	Display OFF

When the display OFF command is executed when in the display all points ON mode, the power save mode is entered. See the section on the power saver for details.

2. Set Display Start Line

Specifies line address (refer to Figure 4) to determine the initial display line, or COM0. The RAM display data becomes the top line of the LCD screen. The higher number of lines in ascending order, corresponding to the duty cycle follows it. This command changes when the line address, smooth scrolling or a page change take place.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	A5	A4	A3	A2	A1	A0

← High-order bit

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
			:			:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

3. Set Page Address

Specifies the page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed. Page address 8 is the display RAM area dedicated to the indicator, and only D0 is valid for data change.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	A3	A2	A1	A0

A3	A2	A1	A0	Page address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

4. Set Column Address

It specifies column address of display RAM. It divides the column address into 4 higher bits and 4 lower bits. Set each of them in succession. When the microprocessor repeats to access the display RAM, the column address counter is incremental during each access until address 132 is accessed. The page address is not changed during this time.

	A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
Higher bits	0	1	0	0	0	0	1	A7	A6	A5	A4
Lower bits	0	1	0	0	0	0	0	A3	A2	A1	A0

A7	A6	A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
								⋮
1	0	0	0	0	0	1	1	131

5. Read Status

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Busy: When high, the NT7532 is busy due to the internal operation or reset. Any command is rejected until BUSY becomes low. The busy check is not required if enough time is provided for each cycle.

ADC: Indicates the relationship between RAM column address and segment drivers. When low, the display is reversed and column address "131-n" corresponds to segment driver n. when high, the display is normal and column address corresponds to segment driver n.

ON/OFF: Indicates whether the display is on or off. When low, the display turns on. When high, the display turns off. This is the opposite of Display ON/OFF command

RESET: Indicates that the initialization is in progress by /RES signal or by reset command. When low, the display is on. When high, the chip is reset.

6. Write Display Data

Write 8-bit data in display RAM. As the column address automatically increments by 1 after each write, the microprocessor can continue to write data of multiple words.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

7. Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address automatically increments by 1 after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after the column address setup. Refer to the display RAM section of the FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

8. ADC Select

Changes the relationship between RAM column address and segment driver. The order of segment driver output pads can be reversed by software. This allows flexible IC layout during LCD module assembly. For details, refer to the column address section of Figure4. When display data is written or read, the column address is incremented by 1 as shown in Figure4.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	D

When D is low, rotation is to the right (normal direction)

When D is high, rotation is to the left (reverse direction)

9. Normal/ Reverse Display

Reverses the Display ON/OFF status without rewriting the contents of the display data RAM.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	D

When D is low, the RAM data is high, being LCD ON potential (normal display)

When D is high, the RAM data is low, being LCD ON potential (reverse display)

10. Entire Display ON

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held.

This command has priority over the Normal/Reverse Display command. When D is low, the normal display status is provided.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	D

When D is high, the entire display ON status is provided. If the Entire Display ON command is executed in the display OFF status, the LCD panel enters Power save mode. Refer to the Power Save section for details.

11. Set LCD Bias

This command selects the voltage bias ratio required for the liquid crystal display.

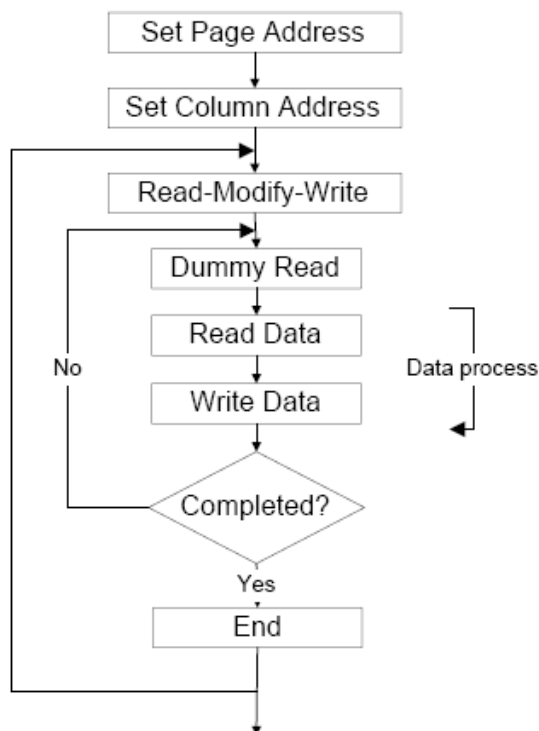
A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Duty			
											1/33	1/49	1/55	1/65
0	1	0	1	0	1	0	0	0	1	0	1/6 bias	1/8 bias	1/8 bias	1/9 bias
											1/5 bias	1/6 bias	1/6 bias	1/7 bias

12. Read-Modify-Write

A pair of Read-Modify-Write and End commands must always be used. Once Read-Modify-Write is issued, the column address is not incremental by Read Display Data command but incremental by Write Display Data command only. It continues until the End command is issued. When the End is issued, the column address returns to the address when Read-Modify-Write is issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed when the cursor is blinking or other events.

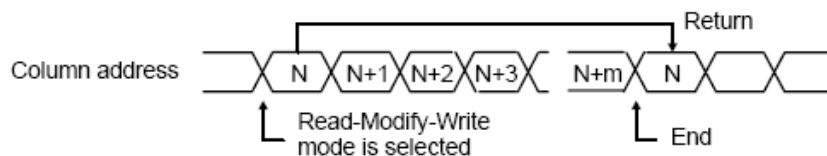
A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

Note: Any command except Read/Write Display Data and Set Column Address can be issued during Read-Modify-Write mode.

Cursor display sequence

13. End

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write is issued).

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0


14. Reset

This command resets the Display Start Line register, Column Address counter, Page Address register, and Common output mode register, the V0 voltage regulator internal resistor ratio register, the Electronic Volume register, the static indicator mode register, the read-modify-write mode register, and the test mode. The Reset command does not affect the contents of display RAM. Refer to the Reset circuit section of Function Description.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

The Reset command cannot initialize the LCD power supply. Only the Reset signal to the /RES pad can initialize the supplies.

15. Output Status Select Register

Applicable to the NT7532. When D is high or low, the scan direction of the COM output pad is selectable. Refer to Output Status Selector Circuit in Function Description for details.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	D	*	*	*

D: Selects the scan direction of COM output pad

D = 0: Normal (COM0 → COM63/53/47/31)

D = 1: Reverse (COM63/53/47/31 → COM0)

*: Invalid bit

16. Set Power Control

Selects one of eight-power circuit functions using a 3-bit register. An external power supply and part of on-chip power circuit can be used simultaneously. Refer to the Power Supply Circuit section of the FUNCTIONAL DESCRIPTION for details.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	A2	A1	A0

When A0 is low, the voltage follower turns off. When A0 is high, it turns on.

When A1 is low, the voltage regulator turns off. When A1 is high, it turns on.

When A2 is low, the voltage booster turns off. When A2 is high, it turns on.

17. V0 Voltage Regulator Internal Resistor Ratio Set

This command sets the V0 voltage regulator internal resistor ratio. For details, see explanation under "The Power Supply Circuits".

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Rb / Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	Small
								0	0	1	
								0	1	0	
									:		:
								1	1	0	
								1	1	1	Large

18. The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal drive voltage V0 through the output from the voltage regulator circuits of the internal liquid crystal power supply.

This command is a double byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

The Electronic Volume Mode Set

When this command is input, the electronic volume register set command is enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	0	0	0	1

Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal voltage V0 assumes one of the 64 voltage levels.

When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	V0
0	1	0	*	*	0	0	0	0	0	0	Small
0	1	0	*	*	0	0	0	0	1	0	
0	1	0	*	*	0	0	0	0	1	1	
0	1	0	*	*			:				:
0	1	0	*	*	1	1	1	1	1	0	
0	1	0	*	*	1	1	1	1	1	1	Large

When the electronic volume function is not used, set D5 - D0 to 100000.

19. Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands.

This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.

The static indicator ON command is a double byte command paired with the static indicator registers, and these commands must be executed one after the other. (The static indicator OFF command is a single byte command.)

Static Indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0	E /RD	R/W/ WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	0	D

D = 0: Static Indicator OFF

D = 1: Static Indicator ON

Static Indicator Register Set

These commands set two bits of data into the static indicator register and are used to set the static indicator into a blinking mode.

A0	E /RD	R/W/ WR	D7	D6	D5	D4	D3	D2	D1	D0	Indicator Display State
0	1	0	*	*	*	*	*	*	0	0	OFF
									0	1	ON (blinking at approximately 0.5 second intervals)
									1	0	ON (blinking at approximately 1 second intervals)
									1	1	ON (constantly on)

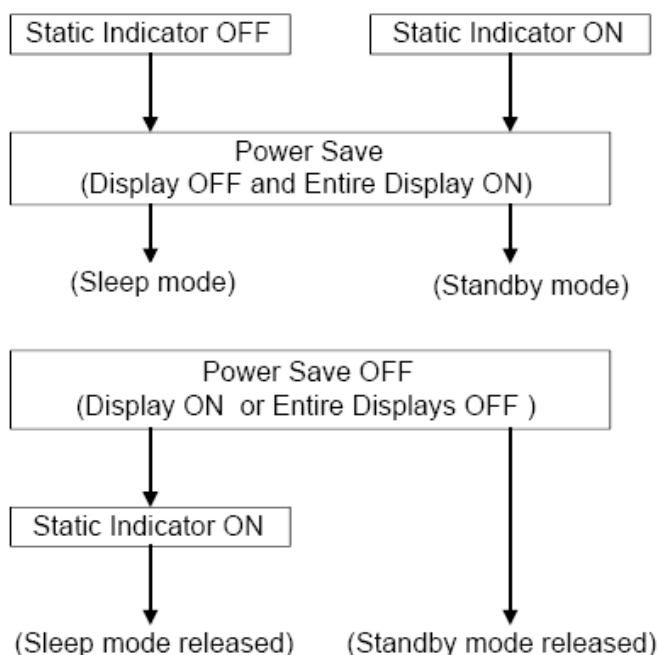
* Disabled bit

20. Power Save (Compound Command)

When all displays are turned on during display off, the Power Save command is issued to greatly reduce current consumption.

If the static indicators are off, the Power Save command makes the system enter sleep mode. If it is on, this command makes the system enter standby mode.

Release the Sleep mode using the both Power Save OFF command (Display ON command or Entire Display OFF command) and Set Indicator On command.



Sleep Mode

This mode stops every operation of the LCD display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

- (1) Stops the oscillator circuit and LCD power supply circuit.
- (2) Stops the LCD drives and outputs the V_{SS} level as the segment/common driver output.
- (3) Holds the display data and operation mode provided before the start of the sleep mode.
- (4) The MPU can access the built-in display RAM.

Standby Mode

Stops the operation of the duty LCD displays system and turns on only the static drive system to reduce current consumption to the minimum level required for the static drive.

The ON operation of the static drive system indicates that the NT7532 is in standby mode. The internal status in the standby mode is as follows:

- (1) Stops the LCD power supply circuit.
- (2) Stops the LCD drive and outputs the V_{SS} level as the segment / common driver output. However, the static drive system still operates.
- (3) Holds the display data and operation mode provided before the start of the standby mode.
- (4) The MPU can access the built-in display RAM.

When the RESET command is issued in the standby mode, the sleep mode is set.

- When an external resistive driver gives the LCD driving voltage level, the current of this resistor must be cut so that it may be fixed to floating or V_{SS} level, prior to or concurrently with causing the NT7532 to go to the sleep mode or standby mode.
- When an external power supply is used, likewise, the function of this external power supply must be stopped so that it may be fixed to floating or V_{SS} level, prior to or concurrently with causing the NT7532 to go into sleep mode or standby mode.

21. NOP

Non-Operation Command

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

22. Test Command

This is the dedicated IC chip test command. It must not be used for normal operation. If the Test command is issued inadvertently set the /RES input to low or issue the Reset command to release the test mode.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	1	*	*	*	*

*: Invalid bit

Cautions: The NT7532 maintains an operation status specified by each command. However, a high level of ambient noise may change the internal operation status. Users must consider how to suppress noise on the package and system or to prevent ambient noise insertion. To prevent a spike in noise, built-in software for periodical status refreshment is recommended.

The test command can be inserted in an unexpected place. Therefore it is recommended to enter the test mode reset command F0h during the refresh sequence.

Command Table

Command	Code											Function	
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0		
(1) Display on/off	0	1	0	1	0	1	0	1	1	1	D	Turns on the LCD panel when high, and turns it off when low	
(2) Set display start line	0	1	0	0	1	Display start address					0	Specifies RAM display line for COM0	
(3) Set page address	0	1	0	1	0	1	1	Page address				0	Sets the display RAM page in Page Address register
(4-1) Set column address 4 higher bits	0	1	0	0	0	0	1	Higher column address				0	Sets 4 higher bits of column address of display RAM in register
(4-2) Set column address 4 lower bits	0	1	0	0	0	0	0	Lower column address				0	Sets 4 lower bits of column address of display RAM in register
(5) Read status	0	0	1	Status				0	0	0	0	0	Reads the status information
(6) Write display data	1	1	0	Write data									Writes data in display RAM
(7) Read display data	1	0	1	Read data									Reads data from display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	D	Sets the display RAM address SEG output correspondence	
(9) Normal/Reverse display	0	1	0	1	0	1	0	0	1	1	D	Normal indication when low, but full indication when high	
(10) Entire display on/off	0	1	0	1	0	1	0	0	1	0	0 1	Selects normal display (0) or Entire Display ON (1)	
(11) Set LCD bias	0	1	0	1	0	1	0	0	0	1	D	Sets LCD drive voltage bias ratio	
(12) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Increments Column Address counter during each write	
(13) End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read-Modify-Write	
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Resets internal functions	
(15) Common output mode select	0	1	0	1	1	0	0	D	*	*	*	Selects COM output scan direction. * Invalid data	
(16) Set power control	0	1	0	0	0	1	0	1	Operation status		0	Selects the power circuit operation mode	
(17) V0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio		0	Select internal resistor ratio (Rb / Ra) mode	
(18) Electronic volume mode set	0	1	0	1	0	0	0	0	0	0	1	Sets the V0 output voltage electronic volume register	
Electronic Volume Register set													*
(19) Set static indicator On/Off	0	1	0	1	0	1	0	1	1	0	D	Sets static indicator On/Off 0: OFF 1: ON	
Set Static indicator register	0	1	0	*	*	*	*	*	*	Mode		Sets the flashing mode	

Command Table (Continued)

Command	Code											Function	
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0		
(20) Power save	-	-	-	-	-	-	-	-	-	-	-	-	Compound command of display OFF and entire display ON
(21) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation	
(22) Test Command	0	1	0	1	1	1	1	*	*	*	*	IC Test command. Do not use!	
(23) Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	Command of test mode reset	

Note: Do not use any other command, or system malfunction may result.

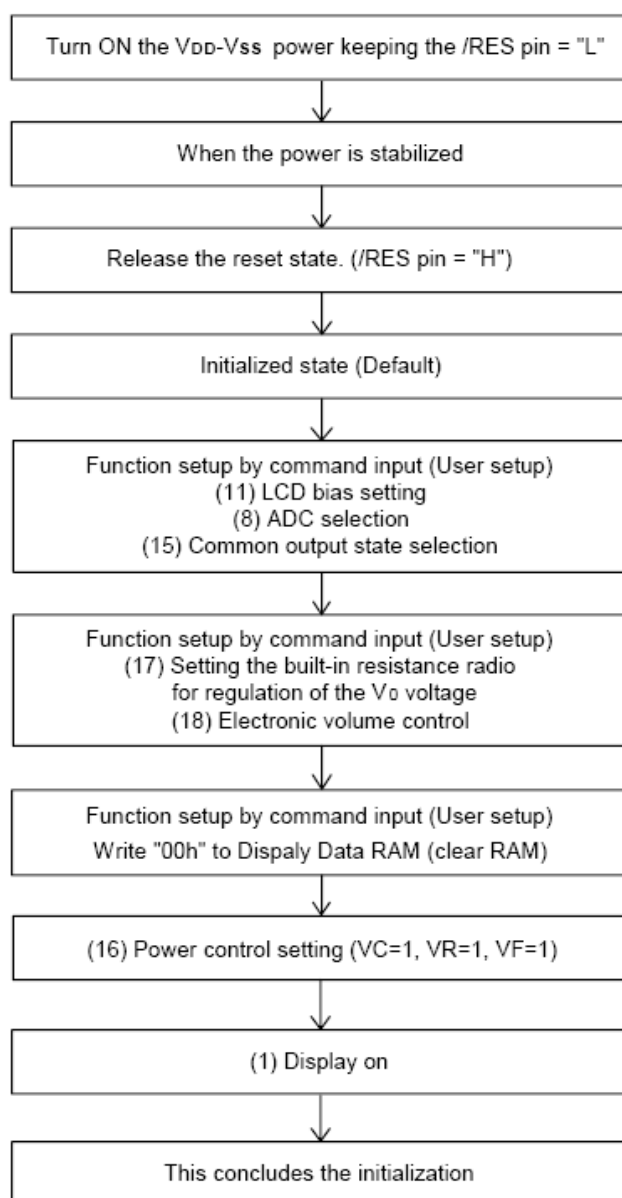
Command Description

Instruction Setup: Reference

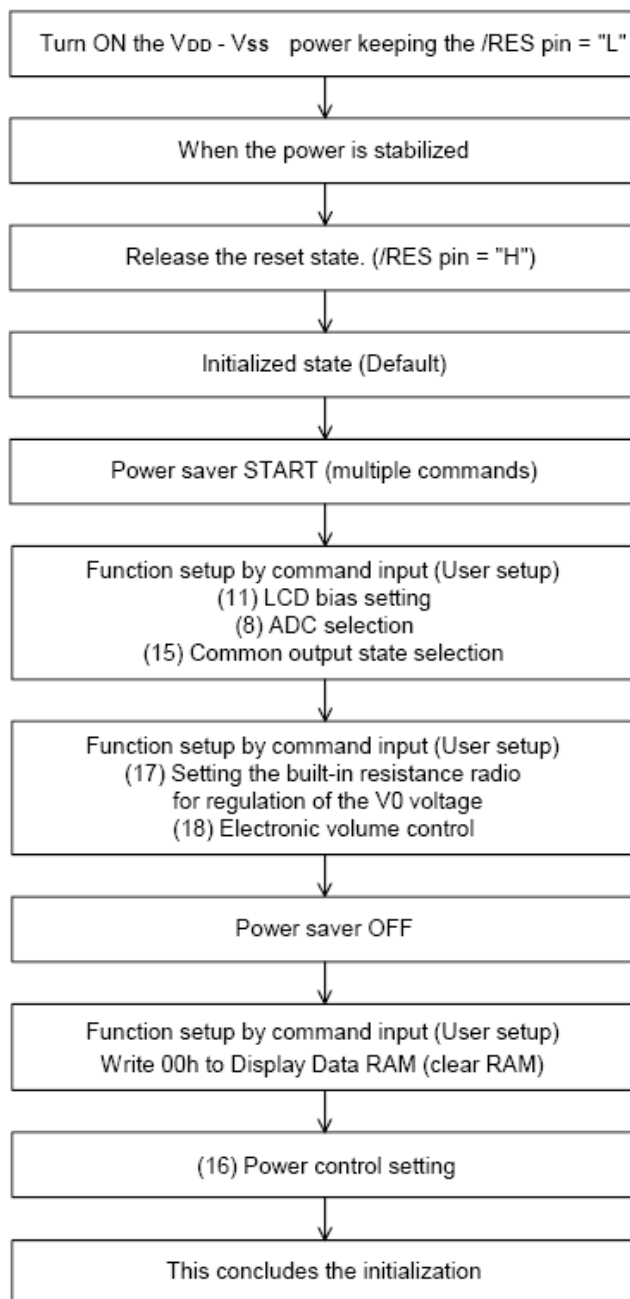
1. Initialization

Note: With this IC, when the power is applied, LCD driving non-selective potentials V2 and V3 (SEG pin) and V1 and V4 (COM pin) are output through the LCD driving output pins SEG and COM. When electric charge is remaining in the smoothing capacitor connecting between the LCD driving voltage output pins (V0 - V4) and the V_{DD} pin, the picture on the display may instantaneously become totally dark when the power is turned on. To avoid such failure, we recommend the following flow sequence when turning on the power.

1.1. When the built-in power is being used immediately after turning on the power:

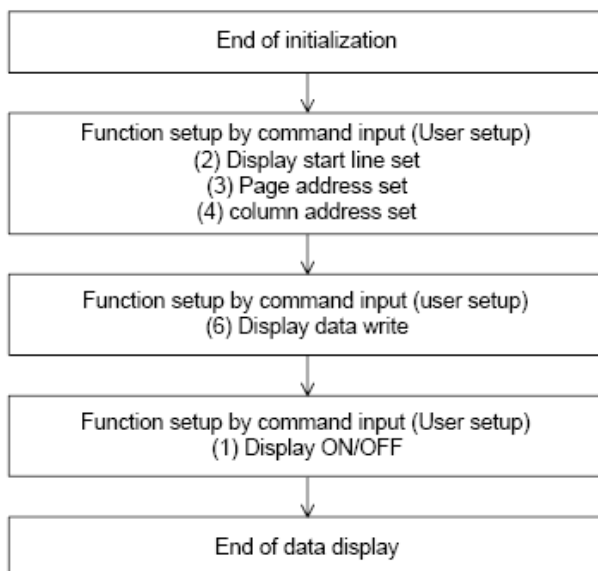


The time of initialization will vary depending on the panel characteristics and capacitance of the smoothing capacitor. Therefore, we suggest you to conduct an operation check using the actual equipment.

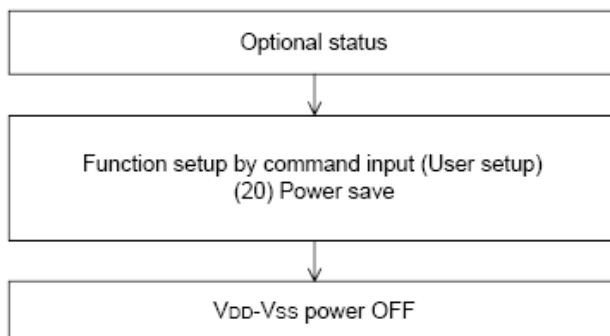
1.2. When the built-in power is not used immediately after turning on the power


The target time of 5ms will vary depending on the panel characteristics and the capacitance of the smoothing capacitor. Therefore, we suggest you conduct an operation check using the actual equipment.

1. Data Display



2. Power OFF



The target time will vary depending on the panel characteristics and capacitance of the smoothing capacitor. Therefore, we suggest you conduct an operation check using the actual equipment.

9. DISPLAY CONTROL FUNCTIONS

Microprocessor Interface

Interface type selection

The NT7532 can transfer data via 8-bit bi-directional data bus (D7 to D0) or via serial data input (SI). When high or low is selected for the parity of P/S pad either 8-bit parallel data input or serial data input can be selected as shown in Table 1. When serial data input is selected, the RAM data cannot be read out.

Table. 1

P/S	Type	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D0 to D5
H	Parallel Input	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D0 to D5
L	Serial Input	/CS1	CS2	A0	-	-	-	SI	SCL	(HZ)

“-” Must always be high or low

Parallel Input

When the NT7532 selects parallel input (P/S = high), the 8080 series microprocessor or 6800 series microprocessor can be selected by causing the C86 pad to go high or low as shown in Table 2.

Table. 2

C86	Type	/CS1	CS2	A0	/RD	/WR	D0 to D7
H	6800 microprocessor bus	/CS1	CS2	A0	E	R/W	D0 to D7
L	8080 microprocessor bus	/CS1	CS2	A0	/RD	/WR	D0 to D7

Data Bus Signals

The NT7532 identifies the data bus signal according to A0, E, R/W(/RD, /WR) signals.

Table. 3

Common	6800 processor (R/W)	8080 processor		Function
		/RD	/WR	
1	1	0	1	Reads display data
1	0	1	0	Writes display data
0	1	0	1	Reads status
0	0	1	0	Writes control data in the internal register. (Command)

Serial Interface (P/S is low)

When the serial interface has been selected (P/S = "L"), then when the chip is in an active state (/CS1 = "L" and CS2 = "H"), the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits of parallel data in the rising edge of the eighth serial clock for processing.

The A0 input is used to determine whether or not the serial data input is displaying data, and when A0 = "L" then the data is command data. The A0 input is read and used for detection every 8th rising edge of the serial clock after the chip becomes active.

Figure 1 is the serial interface signal chart.

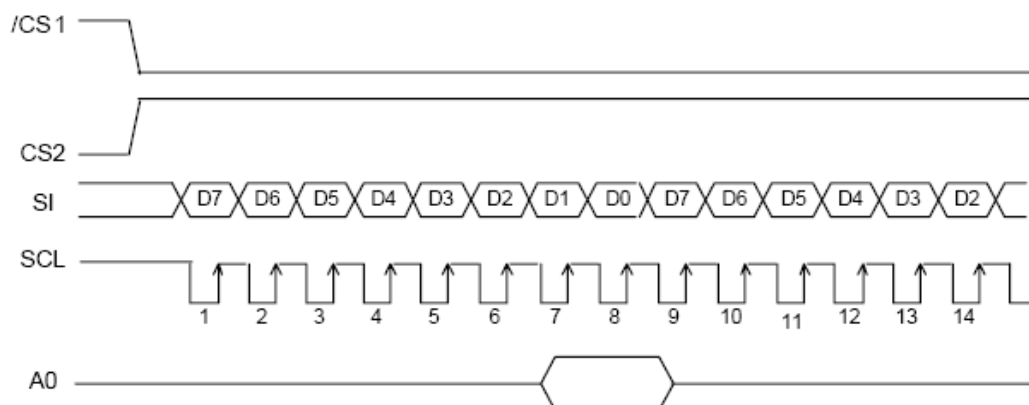


Figure. 1

- When the chip is not active, the shift registers and the counter are reset to their initial states.
- Reading is not possible while in serial interface mode.
- Caution is required on the SCL signal as to line-end reflections and external noise. We recommend the operation be rechecked on the actual equipment.

Chip Select Inputs

The NT7532 has two chip select pads. /CS1 and CS2 can interface to a microprocessor when /CS1 is low and CS2 is high. When these pads are set to any other combination, D0 to D7 are high impedance and A0, E (/RD) and R/W (/WR) inputs are disabled.

When serial input interface is selected, the shift register and counter are reset.

Access to Display Data RAM and Internal Registers

The NT7532 can perform a series of pipeline processing between LSI's using the bus holder of the internal data bus in order to match the operating frequency of display RAM and internal registers with the microprocessor. For example, the microprocessor reads data from display RAM in the first read (dummy) cycle, stores it in the bus holder, and outputs it onto the system bus in the next data read cycle.

Also, the microprocessor temporarily stores display data in the bus holder, and stores it in display RAM until the next data write cycle starts. When viewed from the microprocessor, the NT7532 access speed greatly depends on the cycle time rather than access time to the display RAM (t_{ACC}). This view shows the data transfer speed to / from the microprocessor can increase. If the cycle time is inappropriate, the microprocessor can insert the NOP instruction that is equivalent to the wait cycle setup. However, there is a restriction in the display RAM read sequence. When an address is set, the specified address data is NOT output immediately following the read instruction. The address data is output during the second data read. A single dummy read must be inserted after the address setup and after the write cycle (refer to Figure2).

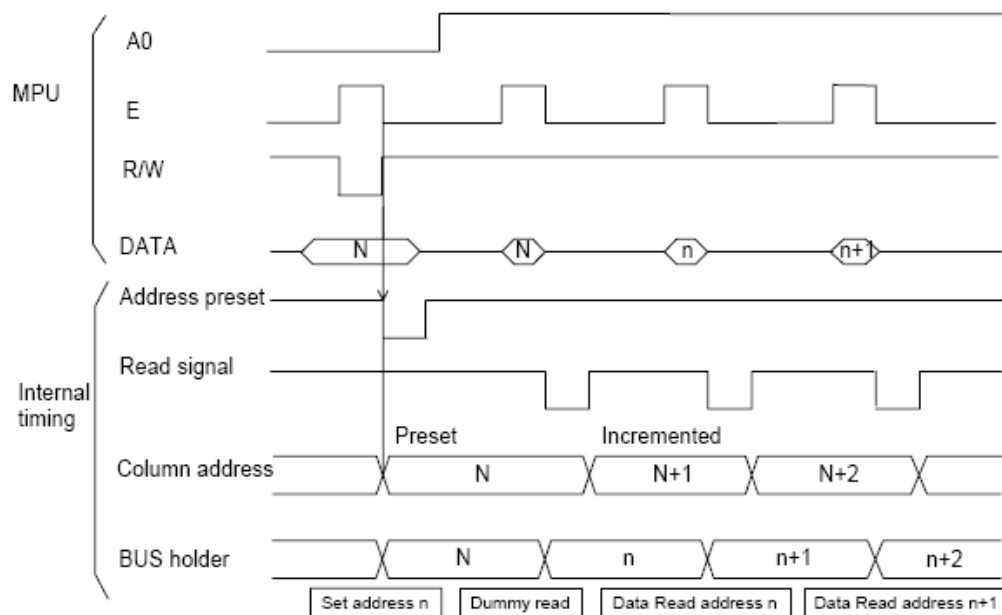


Figure. 2

Busy Flag

When the busy flag is "1" it indicates that the NT7532 chip is running internal processes, and at this time no command aside from a status read will be received. The busy flag is outputted to D7 pad with the read instruction. If the cycle time (tCYC) is maintained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.

Display Data RAM

Display Data RAM

The display data RAM is RAM that stores the dot data for the display. It has a 65(8 page * 8 bit+1)*132 bit structure. It is possible to access the desired bit by specifying the page address and the column address. Because, as is shown in Figure3, the D7 to D0 display data from the MPU corresponds to the liquid crystal display common direction, there are few constraints at the time of display common direction, and there are few constraints at the time of display data transfer when multiple NT7532 chips are used, thus display structures can be created easily and with a high degree of freedom. Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during the liquid crystal display, it will not cause adverse effects on the display (such as flickering).

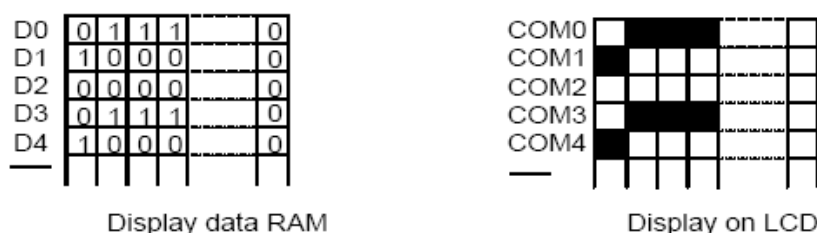


Figure. 3

The Page Address Circuit

As shown in Figure 4, the page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access.

Page address8 (D3, D2, D1, D0 = 1, 0, 0, 0,) is the page for the RAM region used; only display data D0 is used.

The Column Address

As shown in Figure 4, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read / write command. This allows the MPU display data to be accessed continuously. Moreover, the incrimination of column addresses stops with 83H, because the column address is independent of the page address. Thus, when moving, for example, from page0 column 83H to page 1 column 00H, it is necessary to specify both the page address and the column address.

Furthermore, as shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized.

Table. 4

SEG Output	SEG0		SEG131
ADC = "0"	0 (H)→	Column Address	→83 (H)
ADC = "1"	83 (H)←	Column Address	←0 (H)

The Line Address Circuit

The line address circuit, as shown in Table 4, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified. This is the COM0 output when the common output mode is normal and the COM63 output for NT7532, when the common output mode is reversed. The display area is a 65-line area for the NT7532 from the display start line address. If the line addresses are changed dynamically using the display start line address set command, then screen scrolling, page swapping, etc. can be performed.

The Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM.

Because the display normal/reverse status, display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the display data RAM themselves.

The Oscillator Circuit

This is a CR-type oscillator that produces the display clock. The oscillator circuit is only enabled when M/S = "H" and CLS = "H".

When CLS = "L" the oscillation stops, and the display clock is input through the CL terminal.

Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of access to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, there are absolutely no adverse effects (such as flickering) on the display.

Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a driving waveform using a 2-frame alternating current drive method, as is shown in Figure 5, for the liquid crystal drive circuit.

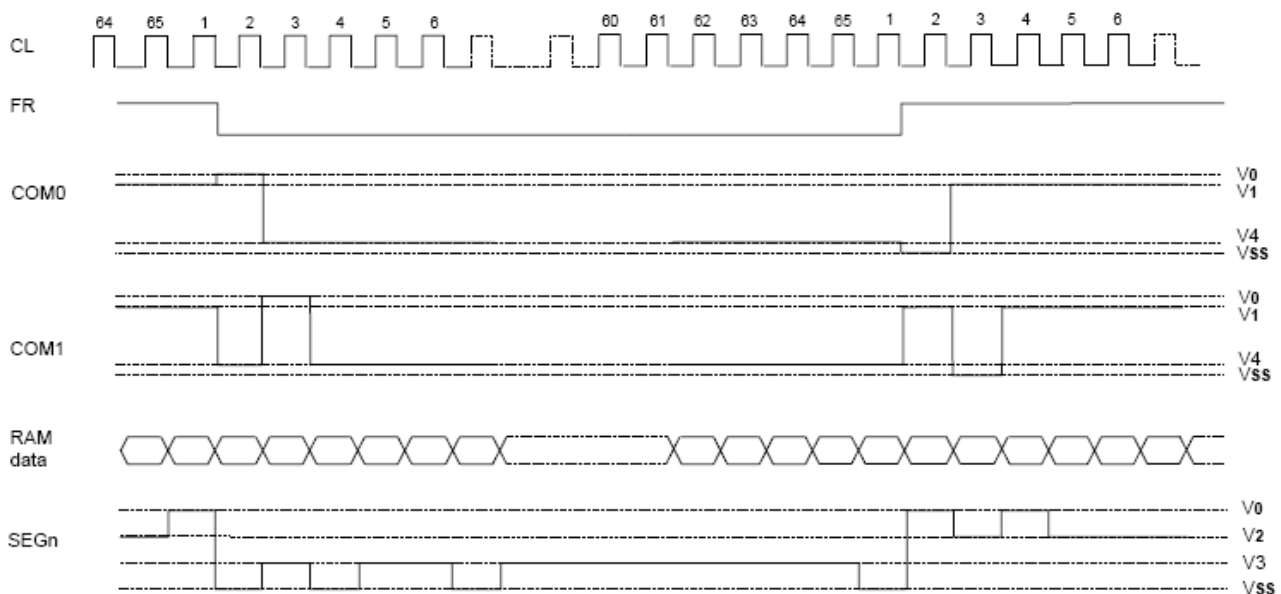


Figure. 5

When multiple NT7532 chips are used, the slave chips must be supplied with the display timing signals (FR, CL, /DOF) from the master chip.

Table 5 shows the status of the FR, CL, and /DOF signals.

Table. 5

Operating Mode		FR	CL	/DOF
Master (M/S = "H")	The internal oscillator circuit is enabled (CLS = "H")	Output	Output	Output
	The internal oscillator circuit is disabled (CLS = "L")	Output	Input	Output
Slave (M/S = "L")	The internal oscillator circuit is disabled (CLS = "H")	Input	Input	Input
	The internal oscillator circuit is disabled (CLS = "L")	Input	Input	Input

Table 6 shows the relationship between oscillation frequency and frame frequency

Table. 6

Duty	Item	f_{CL}	f_{FR}
1/65	On-chip oscillator is used	$f_{osc}/6$	$f_{CL}/(2 \times 65)$
	On-chip oscillator is not used	External input f_{CL}	$f_{CL}/(2 \times 65)$
1/55	On-chip oscillator is used	$f_{osc}/8$	$f_{CL}/(2 \times 55)$
	On-chip oscillator is not used	External input f_{CL}	$f_{CL}/(2 \times 55)$
1/49	On-chip oscillator is used	$f_{osc}/8$	$f_{CL}/(2 \times 49)$
	On-chip oscillator is not used	External input f_{CL}	$f_{CL}/(2 \times 49)$
1/33	On-chip oscillator is used	$f_{osc}/12$	$f_{CL}/(2 \times 33)$
	On-chip oscillator is not used	External input f_{CL}	$f_{CL}/(2 \times 33)$

Common Output Control Circuit

This circuit controls the relationship between the number of common output and specified duty ratio. Common output mode select instruction specifies the scanning direction of the common output pads.

Table. 7

Duty	Status	Common output pads								COMS
		COM [0-15]	COM [16-23]	COM [24-26]	COM [27-36]	COM [37-39]	COM [40-47]	COM [48-63]	COMS	
1/33	Normal	COM[0-15]	NC					COM[16-31]	COMS	
	Reverse	COM[31-16]	NC					COM[15-0]	COMS	
1/49	Normal	COM[0-23]		NC			COM[24-47]		COMS	
	Reverse	COM[47-24]		NC			COM[23-0]		COMS	
1/55	Normal	COM[0-26]			NC		COM[27-53]			COMS
	Reverse	COM[53-27]			NC		COM[26-0]			COMS
1/65	Normal	COM[0-63]								COMS
	Reverse	COM[63-0]								COMS

This is a 197-channel multiplex that generates voltage levels for driving the liquid crystal. The combination of the display data, the COM scans signals, and the FR signal produces the liquid crystal drive voltage output.

Figure 6 shows an example of the SEG and COM output waveforms.

Configuration Setting

The NT7532 has two optional configurations, which are configured by DUTY0, DUTY1

DUTY1, DUTY0	Common	Segment	V1	V2	V3	V4
1, 1	65	132	8/9V0, 6/7V0	7/9V0, 5/7V0	2/9V0, 2/7 V0	1/9V0, 1/7V0
1, 0	55	132	7/8V0, 5/6V0	6/8V0, 4/6V0	2/8V0, 2/6 V0	1/8V0, 1/6V0
0, 1	49	132	7/8V0, 5/6V0	6/8V0, 4/6V0	2/8V0, 2/6 V0	1/8V0, 1/6V0
0, 0	33	132	5/6V0, 4/5V0	4/6V0, 3/5V0	2/6 V0, 2/5V0	1/6V0, 1/5V0

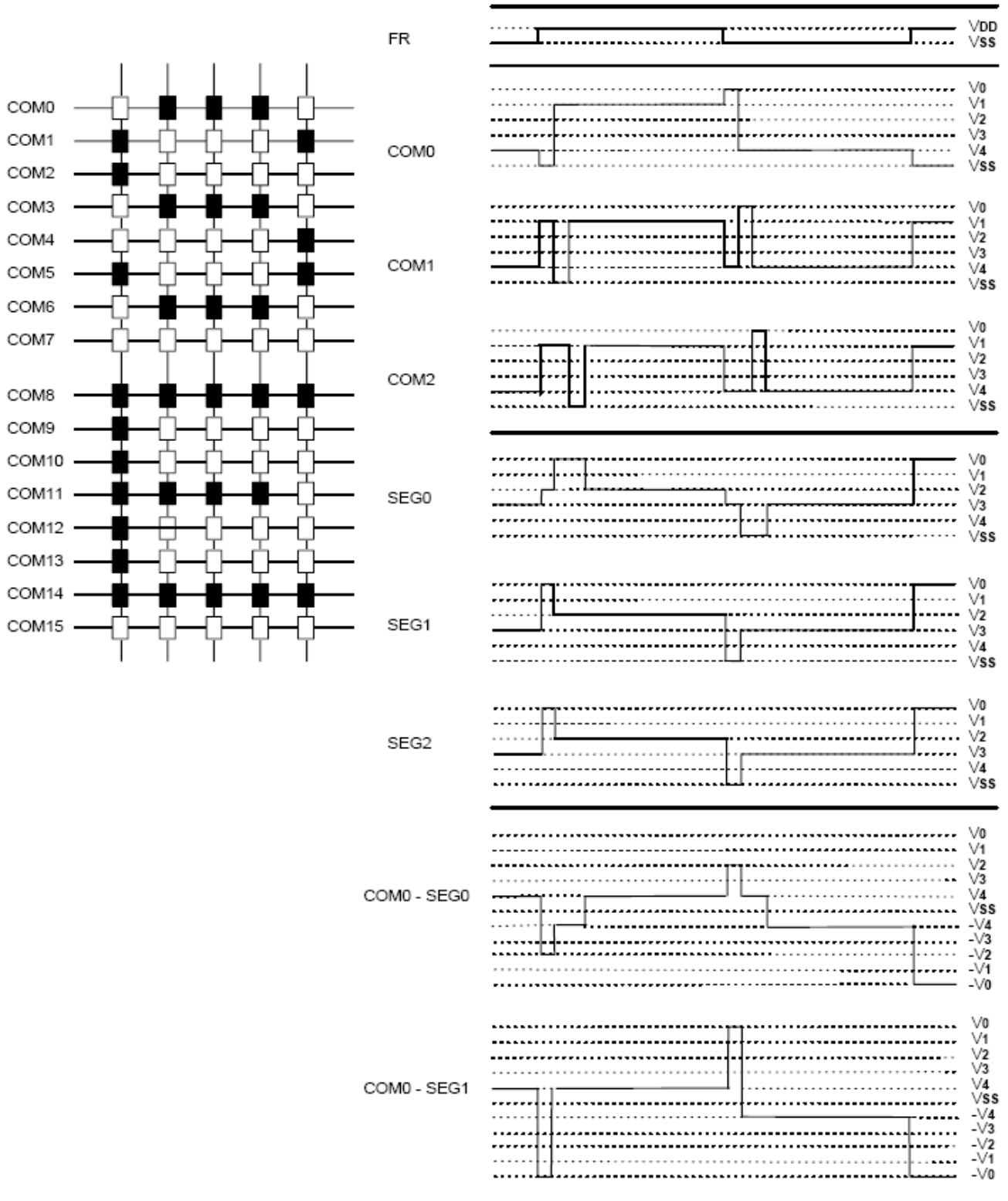


Figure. 6

The Power Supply Circuit

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the liquid crystal drivers. They comprise Booster circuits, voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation.

The power supply circuits can turn the Booster circuits, the voltage regulator circuits, and the voltage follower circuits ON or OFF independently through the use of the Power Control Set commands. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 8 shows the Power Control Set Command 3-bit data control functions, and Table 9 shows combinations as a reference.

Table. 8 The Control Details of Each Bit of the Power Control Set Command

Item	Status	
	"1"	"0"
D2 Booster circuit control bit	ON	OFF
D1 Voltage regulator circuit (V regulator circuit)	ON	OFF
D0 Voltage follower circuit (V/F circuit) control bit	ON	OFF

Table. 9

Use Settings	D2	D1	D0	Step-up circuit	Voltage regulator circuit	V/F circuit	External voltage input	Step-up voltage system terminal
Only the internal power supply is used	1	1	1	O	O	O	V _{DD2}	Used
Only the V regulator circuit and the V/F circuit are used	0	1	1	X	O	O	V _{OUT} , V _{DD2}	Open
Only the V/F circuit is used	0	0	1	X	X	O	V ₀ , V _{DD2}	Open
Only the external power supply is used	0	0	0	X	X	X	V ₀ to V ₄	Open

*The "step-up system terminals" refer to CAP1+, CAP1-, CAP2+, CAP2- and CAP3+.

*While other combinations, not shown above, are also possible, these combinations are not recommended because they have no practical use.

The Step-up Voltage Circuits

Using the step-up voltage circuits within the NT7532 chips it is possible to produce 4X, 3X, 2X step-ups of the V_{DD2} - V_{SS} voltage levels.

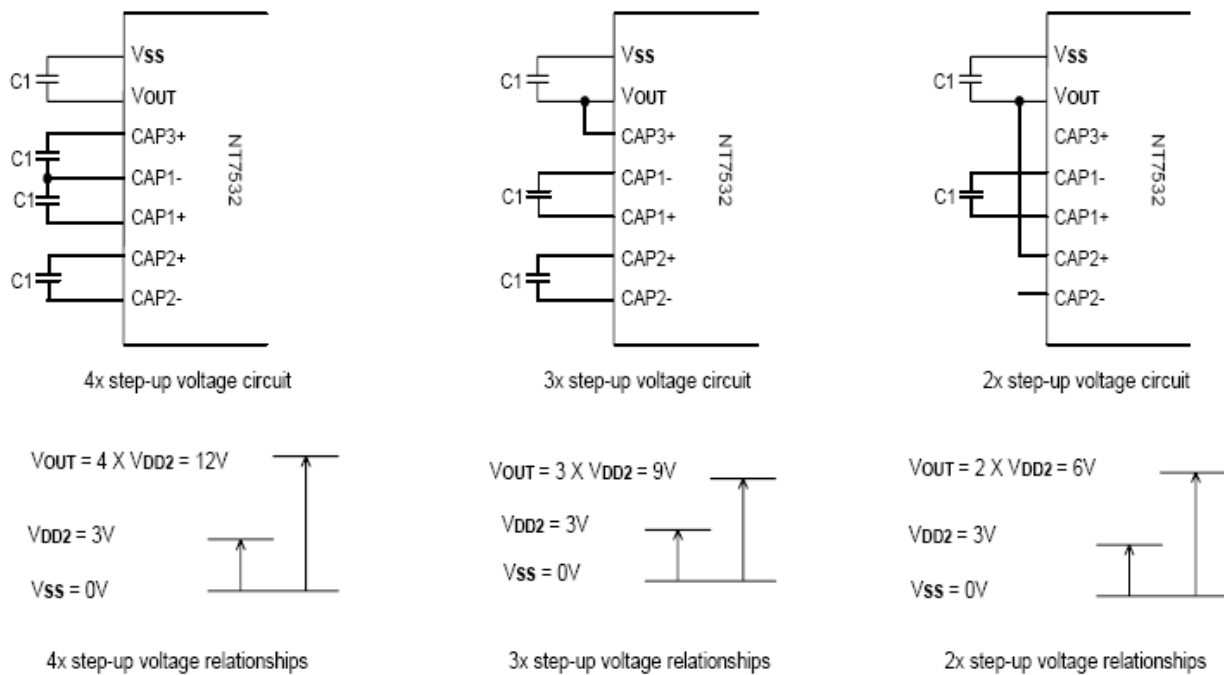


Figure. 7

The Voltage Regulator Circuit

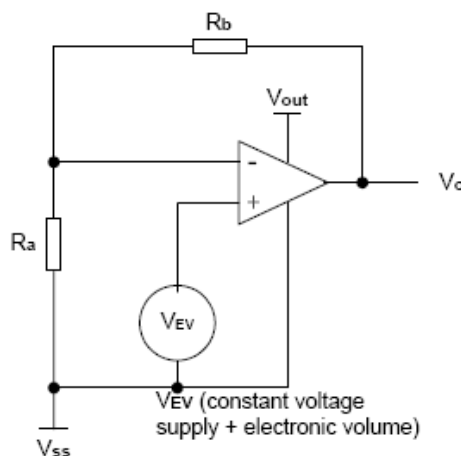
The step-up voltage generated at V_{OUT} outputs the liquid crystal driver voltage V_0 through the voltage regulator circuit. Because the NT7532 chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V_0 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components.

Moreover, in the NT7532, two types of thermal gradients have been prepared as VREG options: (1) approximately $-0.05\%/^{\circ}C$ and (2) external input (supplied to the VEXT terminal).

When the V0 Voltage Regulator Internal Resistors are used

Through the use of the V0 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V0 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V0 voltage can be calculated using equation A-1 over the range where $V0 < V_{OUT}$.

$$V0 = (1 + Rb/Ra) * VEV = (1 + Rb/Ra) * (1 - (63 - \alpha) / 162) * VREG \quad \text{(Equation A-1)}$$



VREG is the IC internal fixed voltage supply, and its voltage at $Ta = 25^{\circ}C$ is shown in Table 10.

Table. 10

Equipment Type	VRS	Thermal Gradient	Units	VREG
Internal power Supply	1	-0.05	%/°C	2.1
External input	0	-	-	VEXT

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume register. Table 10 shows the value for α depending on the electronic volume register settings. Ra/Rb is the V0 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V0 voltage regulator internal resistor ratio set command. The $(1 + Rb/Ra)$ ratio assumes the values shown in Table 11 depending on the 3-bit data settings in the V0 voltage regulator internal resistor ratio register.

Table. 11

D5	D4	D3	D2	D1	D0	α	V0
0	0	0	0	0	0	0	Minimum
0	0	0	0	0	1	1	:
0	0	0	0	1	0	2	:
		:			:	:	:
1	0	0	0	0	0	32 (default)	:
		:			:	:	:
1	1	1	1	1	0	62	:
1	1	1	1	1	1	63	Maximum

V0 voltage regulator internal resistance ratio register value and $(1+R_b/R_a)$ ratio (Reference value)

Table. 12

Register			Equipment Type by Thermal Gradient [Units: %/ °C]	
D2	D1	D0	-0.05 %/°C	VREG External Input
0	0	0	3.0	1.5
0	0	1	3.5	2.0
0	1	0	4.0	2.5
0	1	1	4.5	3.0
1	0	0	5.0	3.5
1	0	1	5.5	4.0
1	1	0	6.0	4.5
1	1	1	6.4	5.0

The V0 voltage as a function of the V0 voltage regulator internal resistor ratio register and the electronic volume register.

Setup example:

When selecting $T_a = 25\text{ °C}$ and $V_0 = 7\text{ V}$ for an NT7532 model on which the temperature compensation is internal, using the equation A-1, the following setup is enabled.

Table. 13

Contents	Register					
	D5	D4	D3	D2	D1	D0
For V0 voltage regulator	-	-	-	0	1	0
Electronic Volume	1	0	0	1	0	1

- When the V0 voltage regulator internal resistors or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands. Moreover, it is necessary to provide a voltage from V_{out} when the Booster circuit is OFF.
- The VR terminal is enabled only when the V0 voltage regulator internal resistors are not used (i.e. the IRS terminal = "L"). When the V0 voltage regulator internal resistors are used (i.e. when the IRS terminal = "H"), then the VR terminal is left open.
- Because the input impedance of the VR terminal is high, it is necessary to take into consideration short leads, shield cables, etc. to handle noise.

The Liquid Crystal Voltage Generator Circuit

The V0 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V1, V2, V3, and V4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V1, V2, V3, and V4 to the liquid crystal drive circuit. 1/9 bias or 1/7 bias for NT7532 can be selected.

High Power Mode

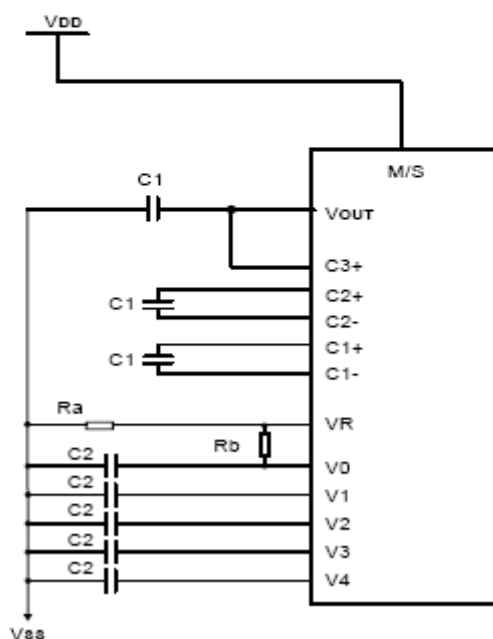
The power supply circuit equipped in the NT7532 chips has very low power consumption (normal mode: /HPM= "H"). However for LCDs or panels with large loads, this low-power power supply may cause the display quality to degrade. When this occurs, setting the /HPM terminal to "L" (high power mode) can improve the quality of the display. We recommend that the display be checked on actual equipment to determine whether or not to use this mode.

Moreover, if the improvement to the display is inadequate even after the high power mode has been set, then it is necessary to add a command sequence when the built-in power supply is turned OFF

To turn off the built-in power supply, follow the command sequence as shown below to turn it off after making the system enter standby mode.

Reference Power Supply Circuit for Driving LCD Panel

-When using all LCD power circuits
(Voltage converter regulator and follower)
(In case of 3X boosting circuit)



Reset Circuit

When the /RES input falls to "L", these LSI reenter their default state. The default settings are shown below:

1. Display OFF
2. Normal display
3. ADC select: Normal display (ADC command D0 = "L")
4. Power control register (D2, D1, D0) = (0, 0, 0,)
5. Register data clear in serial interface
6. LCD power supply bias ratio 1/9 (1/65 duty), 1/8 (1/55, 1/49 duty), 1/6 (1/33 duty)
7. Read modify write OFF
8. Static indicator: OFF
Static indicator register: (D1, D2) = (0, 0)
9. Display start line register set at first line
10. Column address counter set at address 0
11. Page address register set at page 0
12. Common output status normal
13. V0 voltage regulator internal power supply ratio set mode clear:
V0 voltage regulator internal resistor ratio register: (D2, D1, D0) = (1, 0, 0)
14. Electronic volume register set mode clear
Electronic volume register: (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0,)
15. Test mode clear
16. All-indicator-lamps-on OFF (All-indicator-lamps ON/OFF command D0 = "L")
17. Output condition of COM, SEG
COM: V1
SEG: V2

On the other hand, when the reset command is used only default settings 7 to 15 above are put into effect. The MPU interface (Reference Example)", the /RES terminal is connected to the MPU reset terminal, making the chip reinitialize simultaneously with the MPU. At the time of power up, it is necessary to reinitialize using the /RES terminal. Moreover, when the control signal from the MPU is in a high impedance state, there may be an overcurrent condition; therefore, take measures to prevent the input terminal from entering a high impedance state.

In the NT7532, if the internal liquid crystal power supply circuit is not used, then it is necessary to apply an "L" signal to the /RES terminal when the external liquid crystal power supply is applied.

Even though the oscillator circuit operates while the /RES terminal is "L," the display timing generator circuit is stopped, and the FR, FRS, and /DOF terminals are fixed to "H," and the CL pin is fixed to "H" only when the internal oscillator circuit is used. There is no influence on the D0 to D7 terminals.

10. INTERFACE PIN CONNECTIONS

PIN	SYMBOL	I/O	FUNCTION															
1	NC	-	No connect															
2	IRS	I	This terminal selects the resistors for the V0 voltage level adjustment. IRS="H", Use the internal resistors. IRS="L", Do not use the internal resistors. The V0 voltage level is regulated by an external resistive voltage divider that is attached to the VR terminal.															
3	NC	-	No connect															
4	PS	I	This is the parallel data input/serial data input switch terminal P/S="H": Parallel data input P/S="L": Serial data input The following applies depending on the P/S status: <table border="1" data-bbox="387 857 1465 987"> <thead> <tr> <th>P/S</th> <th>Data/Command</th> <th>Data</th> <th>Read/Write</th> <th>Serial clock</th> </tr> </thead> <tbody> <tr> <td>"H"</td> <td>A0</td> <td>D0 to D7</td> <td>/RD, /WR</td> <td>-</td> </tr> <tr> <td>"L"</td> <td>A0</td> <td>SI(D7)</td> <td>Write Only</td> <td>SCL(D6)</td> </tr> </tbody> </table> <p>When P/S="L", D0 to D5 are HZ. D0 to D5 may be "H", "L" or open. /RD(E) and /WR(R/W) are fixed to either "H" or "L". With serial data input, RAM display data reading is not supported.</p>	P/S	Data/Command	Data	Read/Write	Serial clock	"H"	A0	D0 to D7	/RD, /WR	-	"L"	A0	SI(D7)	Write Only	SCL(D6)
P/S	Data/Command	Data	Read/Write	Serial clock														
"H"	A0	D0 to D7	/RD, /WR	-														
"L"	A0	SI(D7)	Write Only	SCL(D6)														
5	C86	I	This is the MPU interface switch terminal C86="H": 6800 Series MPU interface C86="L": 8080 MPU interface															
6	NC	-	No connect															
7	VR	-	Voltage adjustment pad. Applies voltage between V0 and VSS using a resistive divider.															
8	V0	-	LCD driver supplies voltage. The voltage determined by LCD cell is impedance-converted by a resistive driver or an operation amplifier for application. Voltages should be according to the following relationship. $V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS$															
9	V4	-	LCD driver supplies voltage.															
10	V3	-	LCD driver supplies voltage.															
11	V2	-	LCD driver supplies voltage.															
12	V1	-	LCD driver supplies voltage.															
13	NC	-	No connect															
14	CAP2-	-	Capacitor 2- for internal DC/DC voltage converter.															
15	CAP2+	-	Capacitor 2+ for internal DC/DC voltage converter.															
16	CAP1+	-	Capacitor 1+ for internal DC/DC voltage converter.															
17	CAP1-	-	Capacitor 1- for internal DC/DC voltage converter.															
18	CAP3+	-	Capacitor 3+ for internal DC/DC voltage converter.															
19	VOUT	-	DC/DC voltage converter output															

20	VSS	-	Ground pin, connected to 0V
21	VDD	-	Power supply pin for logic .(+3 V)
22	DB7		This is an 8-bit bi-directional data bus that connects to an 8-bit standard MPU data bus. When the serial interface is selected (P/S="L"), then DB7 serves as the serial data input terminal(SI).
23	DB6		This is an 8-bit bi-directional data bus that connects to an 8-bit standard MPU data bus. When the serial interface is selected (P/S="L"), then DB6 serves as the serial clock input terminal(SCL).
24	DB5		This is an 8-bit bi-directional data bus that connects to an 8-bit standard MPU data bus. When the serial interface is selected (P/S="L"), then DB5 are set to high impedance.
25	DB4		This is an 8-bit bi-directional data bus that connects to an 8-bit standard MPU data bus. When the serial interface is selected (P/S="L"), then DB4 are set to high impedance.
26	DB3		This is an 8-bit bi-directional data bus that connects to an 8-bit standard MPU data bus. When the serial interface is selected (P/S="L"), then DB3 are set to high impedance.
27	DB2		This is an 8-bit bi-directional data bus that connects to an 8-bit standard MPU data bus. When the serial interface is selected (P/S="L"), then DB2 are set to high impedance.
28	DB1		This is an 8-bit bi-directional data bus that connects to an 8-bit standard MPU data bus. When the serial interface is selected (P/S="L"), then DB1 are set to high impedance.
29	DB0		This is an 8-bit bi-directional data bus that connects to an 8-bit standard MPU data bus. When the serial interface is selected (P/S="L"), then DB0 are set to high impedance.
30	/RD		When connected to an 8080 MPU, it is active LOW This pad is connected to the /RD signal of the 8080 MPU, and the NT7532 data bus is in an output status when this signal is "L". When connected to a 6800 Series MPU, this is active HIGH, This is used as an enable clock input of the 6800 series MPU.
31	/WR		When connected to an 8080 MPU, it is active LOW This terminal connected to the /WR signal of the 8080 MPU, The signals on the data bus are latched at the rising edge of the /WR signal. When connected to a 6800 Series MPU, this is the read/write control signal input terminal. When R/W = "H": Read When R/W = "L": Write
32	A0		This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0= "H": Indicates that D0 to D7 are display data. A0= "L": Indicates that D0 to D7 are control data.
33	/RST		When /RES is set to "L", the settings are initialized The reset operation is performed by the /RES signal level
34	/CS1		This is the chip select signal. When /CS1 = "L" , then the chip select becomes active, and data/command I/O is enabled.
35	NC	-	No connect
36	NC	-	No connect

11.RELIABILITY
Content of Reliability Test

Environmental Test				
No.	Test Item	Content of Test	Test Condition	Applicable Standard
1	High temperature storage	Endurance test applying the high storage temperature for a long time.	70 °C 200 hrs	
2	Low temperature storage	Endurance test applying the low storage temperature for a long time.	-20 °C 200 hrs	
3	High temperature operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	60 °C 200 hrs	
4	Low temperature operation	Endurance test applying the electric stress under low temperature for a long time.	-10 °C 200 hrs	
5	High temperature Humidity storage	Endurance test applying the high temperature and high humidity storage for a long time.	50 °C , 90,RH 96 hrs	MIL-202E-103B JIS-C5023
6	High temperature Humidity operation	Endurance test applying the electric stress (Voltage & Current) and temperature humidity stress to the element for a long time.	50 °C , 90,RH 96 hrs	MIL-202E-103B JIS-C5023
7	Temperature cycle	Endurance test applying the low and high temperature cycle. <div style="text-align: center;"> $\begin{array}{ccccc} -10^{\circ}\text{C} & & 25^{\circ}\text{C} & & 60^{\circ}\text{C} \\ & \xleftrightarrow{30\text{min.}} & & \xleftrightarrow{5\text{min.}} & \\ & & & & \xleftrightarrow{30\text{min.}} \\ & \xleftarrow{\hspace{10em}} & & & \xrightarrow{\hspace{10em}} \\ & & \text{1 cycle} & & \end{array}$ </div>	-10°C – 60°C 10 cycles	
Mechanical Test				
8	Vibration test	Endurance test applying the vibration during transportation and using.	10-22Hz → 1.5mmp-p 22-500Hz → 1.5G Total 0.5hrs	MIL-202E-201A JIS-C5025 JIS-C7022-A-10
9	Shock test	Constructional and mechanical endurance test applying the shock during transportation.	50G half sign wave 1l msedc 3 times of each direction	MIL-202E-213B
10	Atmospheric pressure test	Endurance test applying the atmospheric pressure during transportation by air.	115 mbar 40 hrs	MIL-202E-105C
Others				
11	Static electricity test	Endurance test applying the electric stress to the terminal.	VS=800V, RS=1.5 k CS=100 pF 1 time	MIL-883B-3015.1

*** Supply voltage for logic system = 3V. Supply voltage for LCD system = Operating voltage at 25°C.

Failure Judgement Criterion

Criterion Item	Test Item No.											Failure Judgment Criterion	
	1	2	3	4	5	6	7	8	9	10	11		
Basic specification													Out of the Basic Specification
Electrical characteristic													Out of the DC and AC Characterstic
Mechanical characterstic													Out of the Mechanical Specification Color change : Out of Limit Apperance Specification
Optical characterstic													Out of the Apperance Standard

12. QUALITY GUARANTEE

Acceptable Quality Level

Each lot should satisfy the quality level defined as follows.

- Inspection method : MIL-STD-105E LEVEL II Normal one time sampling
- AQL

Partition	AQL	Definition
A: Major	0.4%	Functional defective as product
B: Minor	1.5%	Satisfy all functions as product but not satisfy cosmetic standard

Definition of 'LOT'

One lot means the delivery quantity to customer at one time.

Conditions of Cosmetic Inspection

Environmental condition

The inspection should be performed at the 1cm of height from the LCD module under 2 pieces of 40W white fluorescent lamps (Normal temperature 20~25°C and normal humidity 60 ± 15%RH).

Inspection method

The visual check should be performed vertically at more than 30cm distance from the LCD panel.

Driving voltage

The VO value which the most optimal contrast can be obtained near the specified VO in the specification. (Within ± 0.5V of typical value at 25°C.).

13. INSPECTION CRITERIA

13.1 Module Cosmetic Criteria

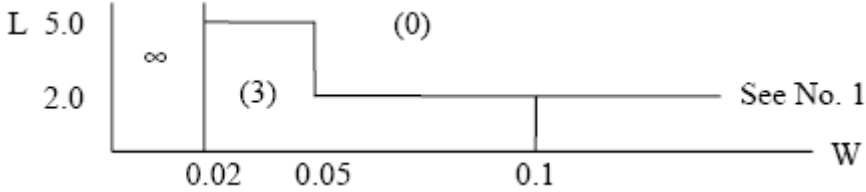
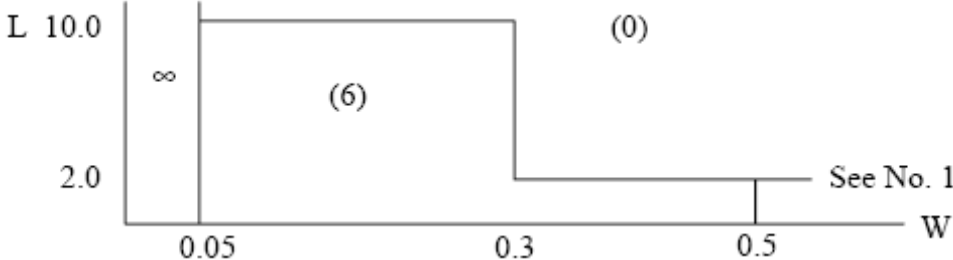
No.	Item	Judgement Criterion	Partition
1	Difference in Spec.	None allowed	Major
2	Pattern peeling	No substrate pattern peeling and floating	Major
3	Soldering defects	No soldering missing No soldering bridge No cold soldering	Major Major Major
4	Resist flaw on substrate	Invisible copper foil (‘0.5mm or more) on substrate pattern	Minor
5	Accretion of metallic Foreign matter	No soldering dust No accretion of metallic foreign matters (Not exceed ‘0.2mm)	Minor Minor
6	Stain	No stain to spoil cosmetic badly	Minor
7	Plate discoloring	No plate fading, rusting and discoloring	Minor
8	Solder amount	a. Soldering side of PCB Solder to form a ‘Filet’ all around the lead. Solder should not hide the lead form perfectly. (too much)	Minor
	1. Lead parts	b. Components side (In case of ‘Through Hole PCB’) Solder to reach the Components side of PCB.	
	2. Flat packages	Either ‘Toe’ (A) or ‘Seal’ (B) of the lead to be covered by ‘Filet’. Lead form to be assume over solder. A B	
	3. Chips	$(3/2) H \geq h \geq (1/2) H$	Minor

13.2 Screen Cosmetic Criteria (Non-Operating)

No.	Defect	Judgement Criterion	Partition										
1	Spots	In accordance with <i>Screen Cosmetic Criteria (Operating) No.1.</i>	Minor										
2	Lines	In accordance with <i>Screen Cosmetic Criteria (Operating) No.2.</i>	Minor										
3	Bubbles in polarizer	<table border="1"> <thead> <tr> <th>Size : d mm</th> <th>Acceptable Qty in active area</th> </tr> </thead> <tbody> <tr> <td>$d \leq 0.3$</td> <td>Disregard</td> </tr> <tr> <td>$0.3 < d \leq 1.0$</td> <td>3</td> </tr> <tr> <td>$1.0 < d \leq 1.5$</td> <td>1</td> </tr> <tr> <td>$1.5 < d$</td> <td>0</td> </tr> </tbody> </table>	Size : d mm	Acceptable Qty in active area	$d \leq 0.3$	Disregard	$0.3 < d \leq 1.0$	3	$1.0 < d \leq 1.5$	1	$1.5 < d$	0	Minor
Size : d mm	Acceptable Qty in active area												
$d \leq 0.3$	Disregard												
$0.3 < d \leq 1.0$	3												
$1.0 < d \leq 1.5$	1												
$1.5 < d$	0												
4	Scratch	In accordance with spots and lines operating cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor										
5	Allowable density	Above defects should be separated more than 30mm each other.	Minor										
6	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Back-lit type should be judged with back-lit on state only.	Minor										
7	Contamination	Not to be noticeable.	Minor										

13.3. Screen Cosmetic Criteria (Operating)

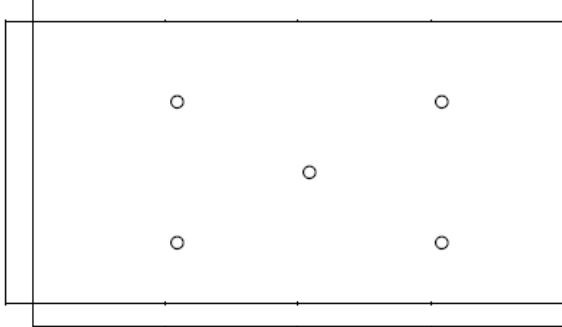
No.	Defect	Judgement Criterion	Partition																				
1	Spots	<p>A) Clear Note :</p> <table border="1"> <thead> <tr> <th>Size : d mm</th> <th>Acceptable Qty in active area</th> </tr> </thead> <tbody> <tr> <td>$d \leq 0.1$</td> <td>Disregard</td> </tr> <tr> <td>$0.1 < d \leq 0.2$</td> <td>3</td> </tr> <tr> <td>$0.2 < d \leq 0.3$</td> <td>2</td> </tr> <tr> <td>$0.3 < d$</td> <td>0</td> </tr> </tbody> </table> <p>Including pin holes and defective dots which must be within one pixel size.</p> <p>B) Unclear Size :</p> <table border="1"> <thead> <tr> <th>Size : d mm</th> <th>Acceptable Qty in active area</th> </tr> </thead> <tbody> <tr> <td>$d \leq 0.2$</td> <td>Disregard</td> </tr> <tr> <td>$0.2 < d \leq 0.5$</td> <td>6</td> </tr> <tr> <td>$0.5 < d \leq 0.7$</td> <td>2</td> </tr> <tr> <td>$0.7 < d$</td> <td>0</td> </tr> </tbody> </table>	Size : d mm	Acceptable Qty in active area	$d \leq 0.1$	Disregard	$0.1 < d \leq 0.2$	3	$0.2 < d \leq 0.3$	2	$0.3 < d$	0	Size : d mm	Acceptable Qty in active area	$d \leq 0.2$	Disregard	$0.2 < d \leq 0.5$	6	$0.5 < d \leq 0.7$	2	$0.7 < d$	0	Minor
Size : d mm	Acceptable Qty in active area																						
$d \leq 0.1$	Disregard																						
$0.1 < d \leq 0.2$	3																						
$0.2 < d \leq 0.3$	2																						
$0.3 < d$	0																						
Size : d mm	Acceptable Qty in active area																						
$d \leq 0.2$	Disregard																						
$0.2 < d \leq 0.5$	6																						
$0.5 < d \leq 0.7$	2																						
$0.7 < d$	0																						

2	Lines	<p>A)Clear</p>  <p>Note : () - Acceptable Qty in active area L -Length (mm) W - Width (mm) ∞ - Disregard</p> <p>B) Unclear</p> 	Minor
---	-------	--	-------

'Clear' = The shade and size are not changed by VO.

'Unclear' = The shade and size are changed by VO.

13.4. Screen Cosmetic Criteria (Operating) (Continued)

No.	Defect	Judgement Criterion	Partition
3	Rubbing line	Not to be noticeable.	
4	Allowable density	Above defects should be separated more than 10mm each other.	Minor
5	Rainbow	Not to be noticeable.	Minor
6	Dot size	To be 95% ~ 105% of the dot size (Typ.) in drawing. Partial defects of each dot (ex. pin-hole) should be treated as 'Spot'. (see <i>Screen Cosmetic Criteria (Operating) No.1</i>)	Minor
7	Uneven brightness (only back-lit type module)	<p>Uneven brightness must be $B_{MAX} / B_{MIN} \leq 2$</p> <ul style="list-style-type: none"> - BMAX : Max. value by measure in 5 points - BMIN : Min. value by measure in 5 points <p>Divide active area into 4 vertically and horizontally. Measure 5 points shown in the following figure.</p>  <p>○ : Measuring points</p>	Minor

Note :

- (1) Size : $d = (\text{long length} + \text{short length}) / 2$
- (2) The limit samples for each item have priority.

(3) Complexed defects are defined item by item, but if the number of defects are defined in above table, the total number should not exceed 10.

- (4) In case of 'concentration', even the spots or the lines of 'disregarded' size should not allowed.

Following three situations should be treated as 'concentration'.

- 7 or over defects in circle of '5mm.
- 10 or over defects in circle of '10mm.
- 20 or over defects in circle of '20mm.

14. PRECAUTIONS FOR USING LCD MODULES

Handing Precautions

- (1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it or impact.
- (2) If the display panel is damaged and the liquid crystal substance leaks out, be sure not to get any in your mouth. If the substance contacts your skin or clothes, wash it off using soap and water.
- (3) Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- (4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.
- (5) If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents :
 - Isopropyl alcohol
 - Ethyl alcohol
- (6) Solvents other than those above-mentioned may damage the polarizer. Especially, do not use the following.
 - Water
 - Ketone
 - Aromatic solvents
- (7) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.
- (8) Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the IO cable or the backlight cable.
- (9) Do not attempt to disassemble or process the LCD module.
- (10) NC terminal should be open. Do not connect anything.
- (11) If the logic circuit power is off, do not apply the input signals.
- (12) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
 - Be sure to ground the body when handling the LCD modules.

- Tools required for assembling, such as soldering irons, must be properly grounded.
- To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions.

- The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

Storage Precautions

When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags (avoid high temperature, high humidity and low temperatures below 0°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

Others

Liquid crystals solidify under low temperature (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subject to a low temperature.

If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.

To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity etc., exercise care to avoid holding the following sections when handling the modules.

- Exposed area of the printed circuit board.
- Terminal electrode sections.

15. USING LCD MODULES

Liquid Crystal Display Modules

LCD is composed of glass and polarizer. Pay attention to the following items when handling.

- (1) Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.
- (2) Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead (glass, tweezers, etc.).
- (3) N-hexane is recommended for cleaning the adhesives used to attach front/rear polarizers and reflectors made of organic substances which will be damaged by chemicals such as acetone, toluene, ethanol and isopropylalcohol.
- (4) When the display surface becomes dusty, wipe gently with absorbent cotton or other soft material like chamois soaked in petroleum benzin. Do not scrub hard to avoid damaging the display surface.
- (5) Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.
- (6) Avoid contacting oil and fats.
- (7) Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizers. After products are tested at low temperature they must be warmed up in a container before coming

is contacting with room temperature air.

(8) Do not put or attach anything on the display area to avoid leaving marks on.

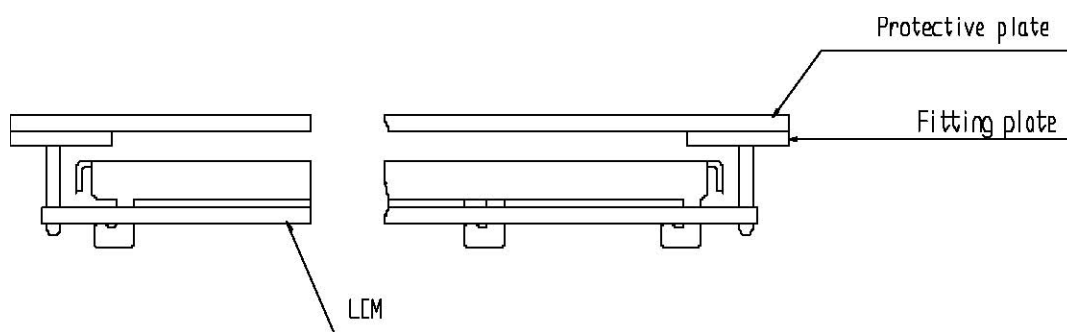
(9) Do not touch the display with bare hands. This will stain the display area and degrade insulation between terminals (some cosmetics are determined to the polarizers).

(10) As glass is fragile. It tends to become or chipped during handling especially on the edges. Please avoid dropping or jarring.

Installing LCD Modules

The hole in the printed circuit board is used to fix LCM as shown in the picture below. Attend to the following items when installing the LCM.

(1) Cover the surface with a transparent protective plate to protect the polarizer and LC cell.



(2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be 0.1mm.

Precaution for Handling LCD Modules

Since LCM has been assembled and adjusted with a high degree of precision, avoid applying excessive shocks to the module or making any alterations or modifications to it.

(1) Do not alter, modify or change the the shape of the tab on the metal frame.

(2) Do not make extra holes on the printed circuit board, modify its shape or change the positions of components to be attached.

(3) Do not damage or modify the pattern writing on the printed circuit board.

(4) Absolutely do not modify the zebra rubber strip (conductive rubber) or heat seal connector.

(5) Except for soldering the interface, do not make any alterations or modifications with a soldering iron.

(6) Do not drop, bend or twist LCM.

Electro-Static Discharge Control

Since this module uses a CMOS LSI, the same careful attention should be paid to electrostatic discharge as for an ordinary CMOS IC.

(1) Make certain that you are grounded when handling LCM.

(2) Before remove LCM from its packing case or incorporating it into a set, be sure the module and your body have the same electric potential.

(3) When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not

leak.

(4) When using an electric screwdriver to attach LCM, the screwdriver should be of ground potentiality to minimize as much as possible any transmission of electromagnetic waves produced sparks coming from the commutator of the motor.

(5) As far as possible make the electric potential of your work clothes and that of the work bench the ground potential.

(6) To reduce the generation of static electricity be careful that the air in the work is not too dried. A relative humidity of 50%~60% is recommended.

Precaution for soldering to the LCM

(1) Observe the following when soldering lead wire, connector cable and etc. to the LCM.

- Soldering iron temperature : 280℃ ~ 300℃.
- Soldering time : 3-4 sec.
- Solder : eutectic solder.

If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage due to flux spatters.

(2) When soldering the electroluminescent panel and PC board, the panel and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.

(3) When remove the electroluminescent panel from the PC board, be sure the solder has completely melted, the soldered pad on the PC board could be damaged.

Precautions for Operation

(1) Viewing angle varies with the change of liquid crystal driving voltage (VO). Adjust VO to show the best contrast.

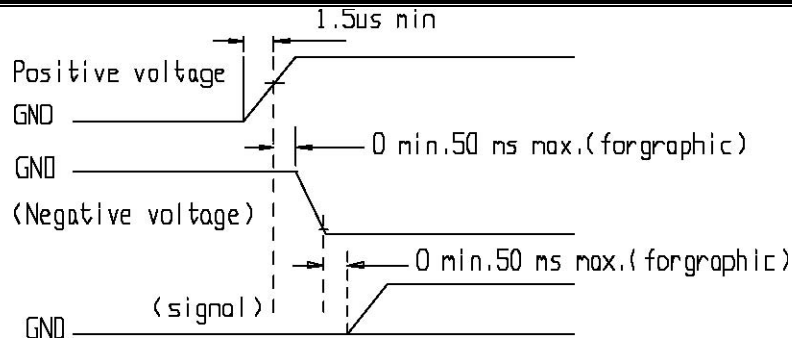
(2) Driving the LCD in the voltage above the limit shortens its life.

(3) Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD will be out of the order. It will recover when it returns to the specified temperature range.

(4) If the display area is pushed hard during operation, the display will become abnormal. However, it will return to normal if it is turned off and then back on.

(5) Condensation on terminals can cause an electrochemical reaction disrupting the terminal circuit. Therefore, it must be used under the relative condition of 40℃ , 50% RH.

(6) When turning the power on, input each signal after the positive/negative voltage becomes stable.



Storage

When storing LCDs as spares for some years, the following precaution are necessary.

- (1) Store them in a sealed polyethylene bag. If properly sealed, there is no need for dessicant.
- (2) Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature between 0°C and 35°C.

(3) The polarizer surface should not come in contact with any other objects. (We advise you to store them in the container in which they were shipped.)

Safety

(1) It is recommended to crush damaged or unnecessary LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.

(2) If any liquid leaks out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

Limited Warranty

Unless agreed between YAOYU and customer, YAOYU will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with YAOYU LCD acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects must be returned to YAOYU within 90 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of YAOYU limited to repair and/or replacement on the terms set forth above. YAOYU will not be responsible for any subsequent or consequential events.

Return LCM under warranty

No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are :

- Broken LCD glass.
- PCB eyelet's damaged or modified.
- PCB conductors damaged.
- Circuit modified in any way, including addition of components.
- PCB tampered with by grinding, engraving or painting varnish.
- soldering to or modifying the bezel in any manner.

Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB eyelet's, conductors and terminals.